SpaceAGE Bus:
New Avionics Building Block Concept

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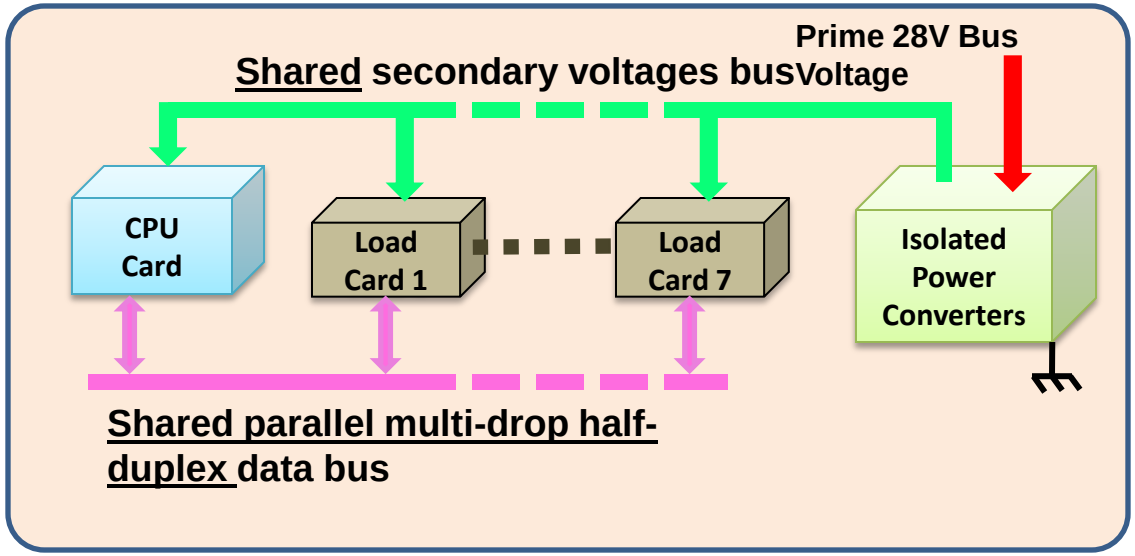
Signal Buses Traditional Approach: Electrical

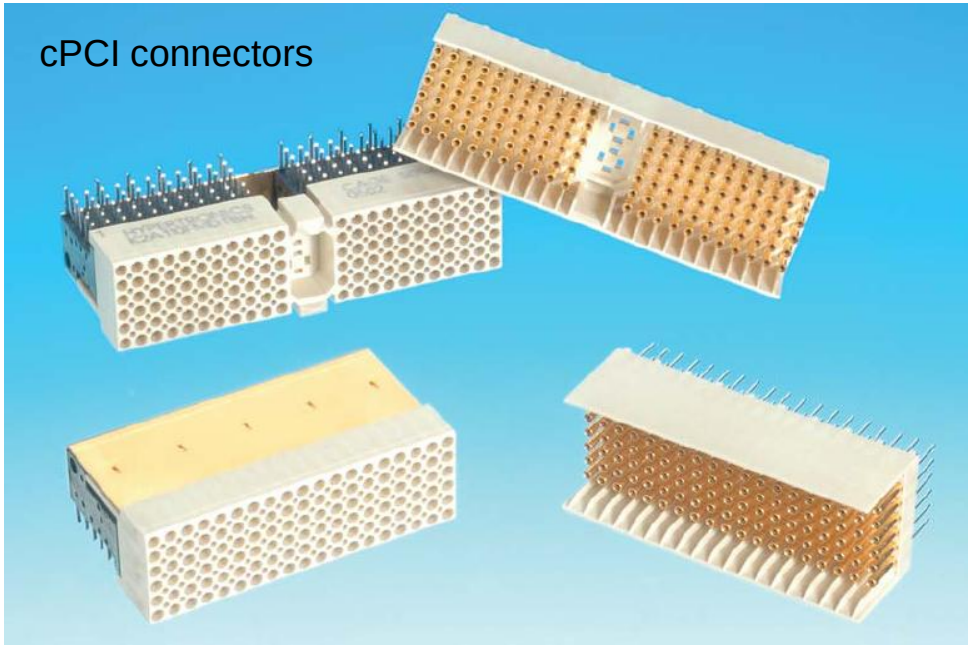
- Custom and/or Euro Card form factor (typically 6U or 3U)
  - Single sided or double sided boards
- Parallel Printed Wiring Board backplane (derived from commercial world)
- Some custom signals added to standard signal set making interchangeability difficult
- All Cards communicate with CPU/Hub through half duplex interface only one at a time
- Line fault isolation is difficult to achieve because of shared power and bus signals
- No EMI isolation between cards

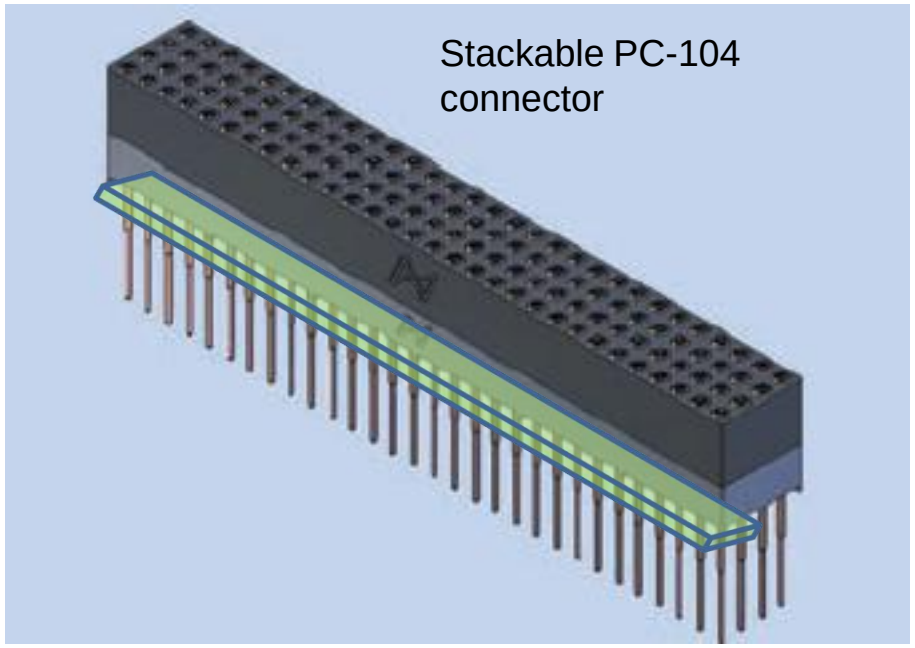


Classical C&DH Architecture

Signal Buses Traditional Approach: Connectors

- Hundreds of pins
  - High mate / de-mate forces
  - Stackable connectors are not solderable (lower reliability in vibration)
- Not impedance matched
  - Very difficult to communicate on high speeds
- Difficult alignment and mount

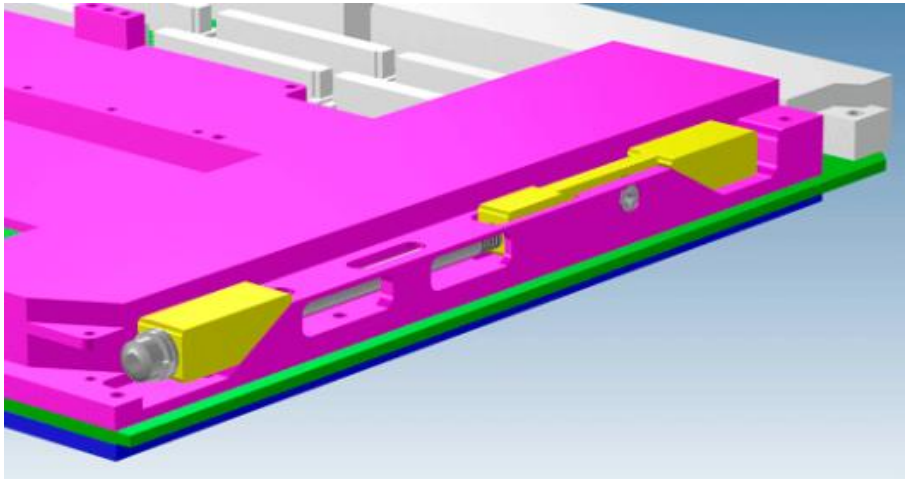


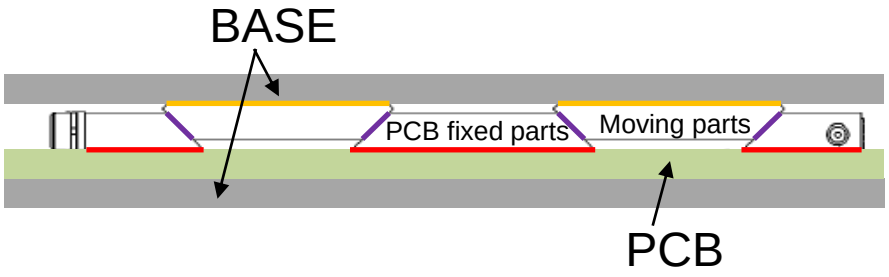


Signal Buses Traditional Approach: Mechanical

- Custom Enclosure design with card faceplate integrated with card
  - Only 1 available side for user interface connectors
- Wedge locks for card locking and heat dissipation path:
  - Difficult inspection of installed cards: may not be possible at all
  - Possibility of “shaving” wedges during insertion: small metal particles in space
- Fixed distance between cards
  - Problems with tall components or dual side assembly

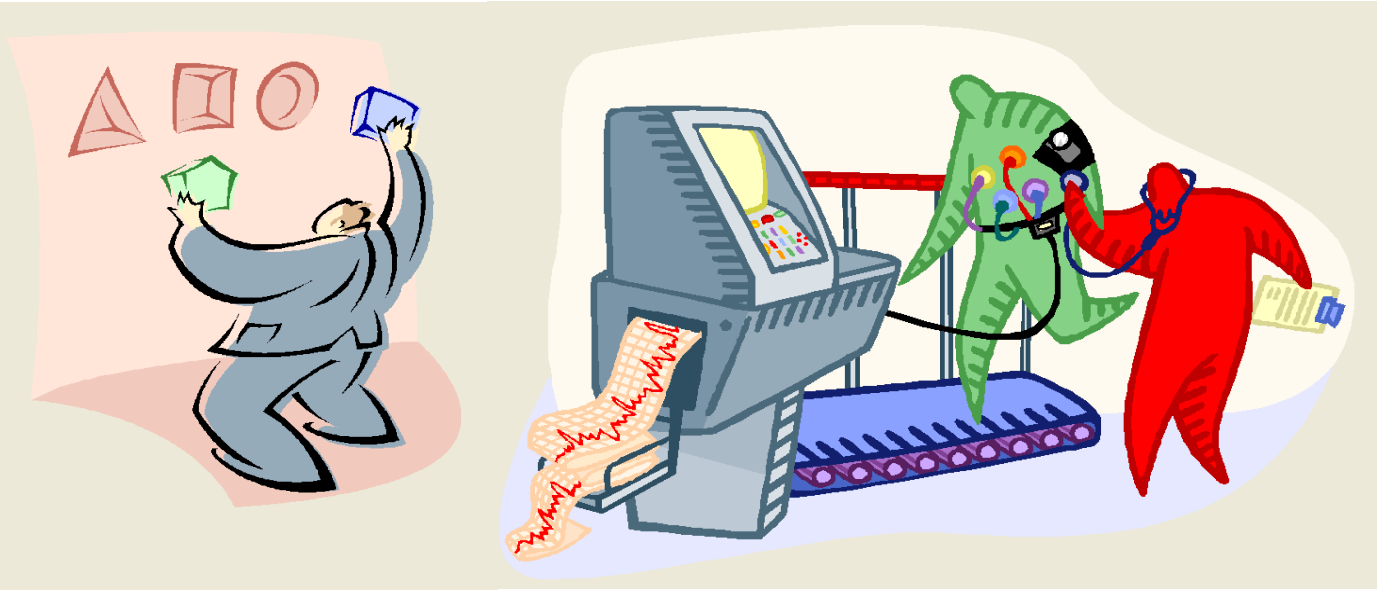
Wedge lock assembly





Signal Buses Traditional Approach: Qualification

- Incompatibility of cards from various vendors
  - Very strong engineering system control is required
  - Some vendors use this to “tie” customers exclusively to their products
  - Sometimes sophisticated rework and redesign is required to match all cards
- Modules are integrated into enclosure are only functionally tested
  - Cards come environmentally untested from vendors: additional testing (EMI/EMC, thermal, vibration) on box level is required



Design Goals

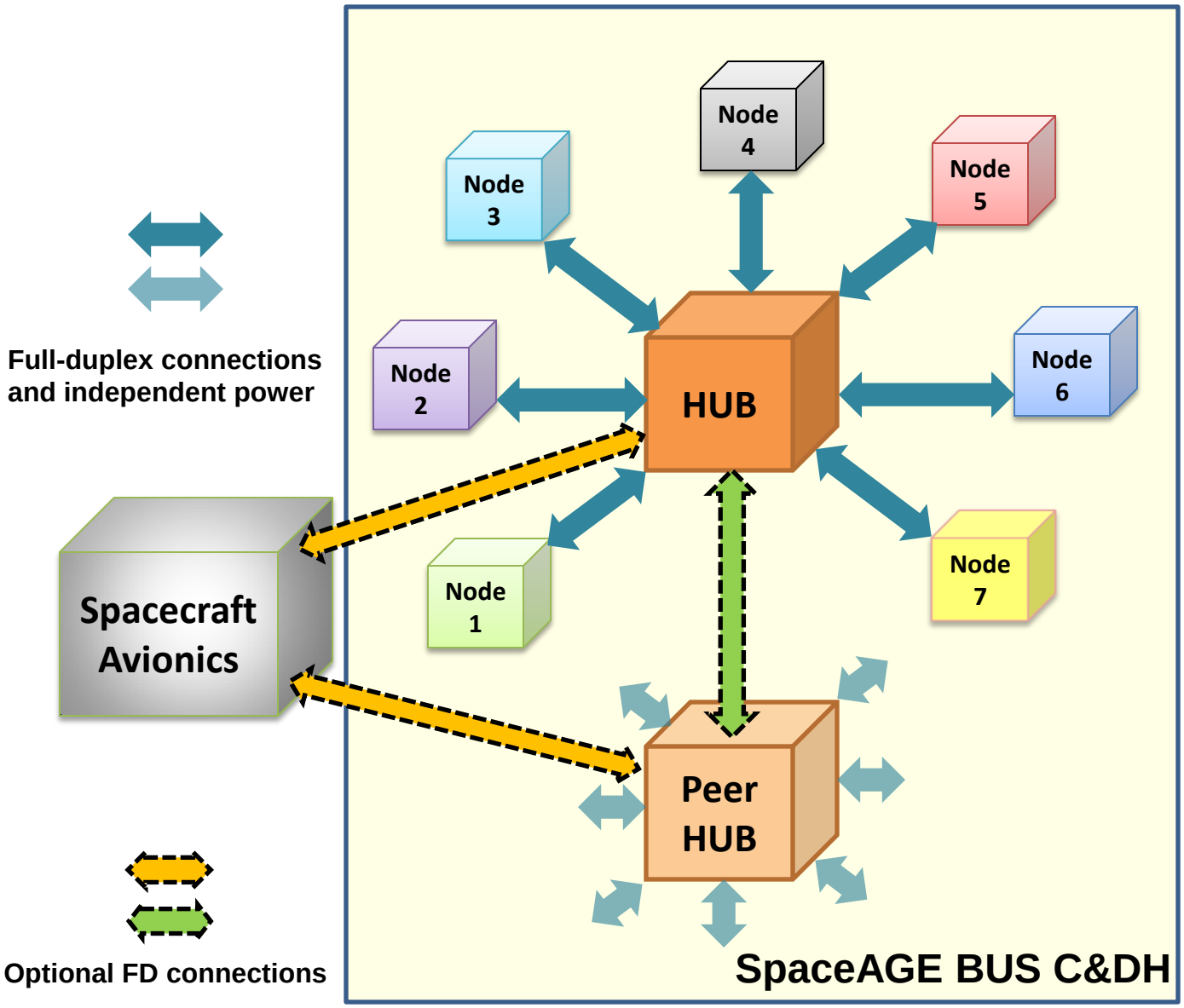
- Create architecture suitable for 90% of space missions
- Reduce costs avionics system development
  - Through significant reduction of Non-Recurring Engineering (NRE)
  - Through standardization of avionic's electrical and mechanical interfaces
- Simplify electrical interfaces by adopting:
  - Serial communications interface
    - Eliminate mechanical tolerances between backplane connectors and boards
    - Increase system reliability by reducing number of signals
  - Single voltage power distribution
    - Higher voltages to reduce current and eliminate voltage margin concerns
  - Minimal set of commonly used signals
  - Interconnection through a star architecture
    - Common or Central module – HUB
    - Peripheral or User module – NODE

- Simplify mechanical interfaces by adopting:
  - Modular and variable length slot mechanical enclosure concept using card frames (slices) where:
    - Each Printed Wiring Board (PWB) includes its own portion of the mechanical chassis
    - Improvement of thermal design – eliminates wedge locks as thermal path
    - Qualifies modules (slices) for EMI/EMC and thermal requirements
    - Significantly reduces tolerance of mechanical design

Major System Requirements

- High speed communication links
  - Compatibility with high speed (gigabit) serial protocol
- Power distribution
- Reliability
  - module-to-module isolation
  - Support Redundancy schemes
- Ease of implementation
  - Minimal compatibility requirements
  - Simple predefined interfaces
- Ease of expansion
  - Up to 7 NODE modules in same chassis (8 or 9 modules total including HUB module(s))
  - At least 1 surface reserved for user connectors

Proposed SpaceAGE Bus Architecture



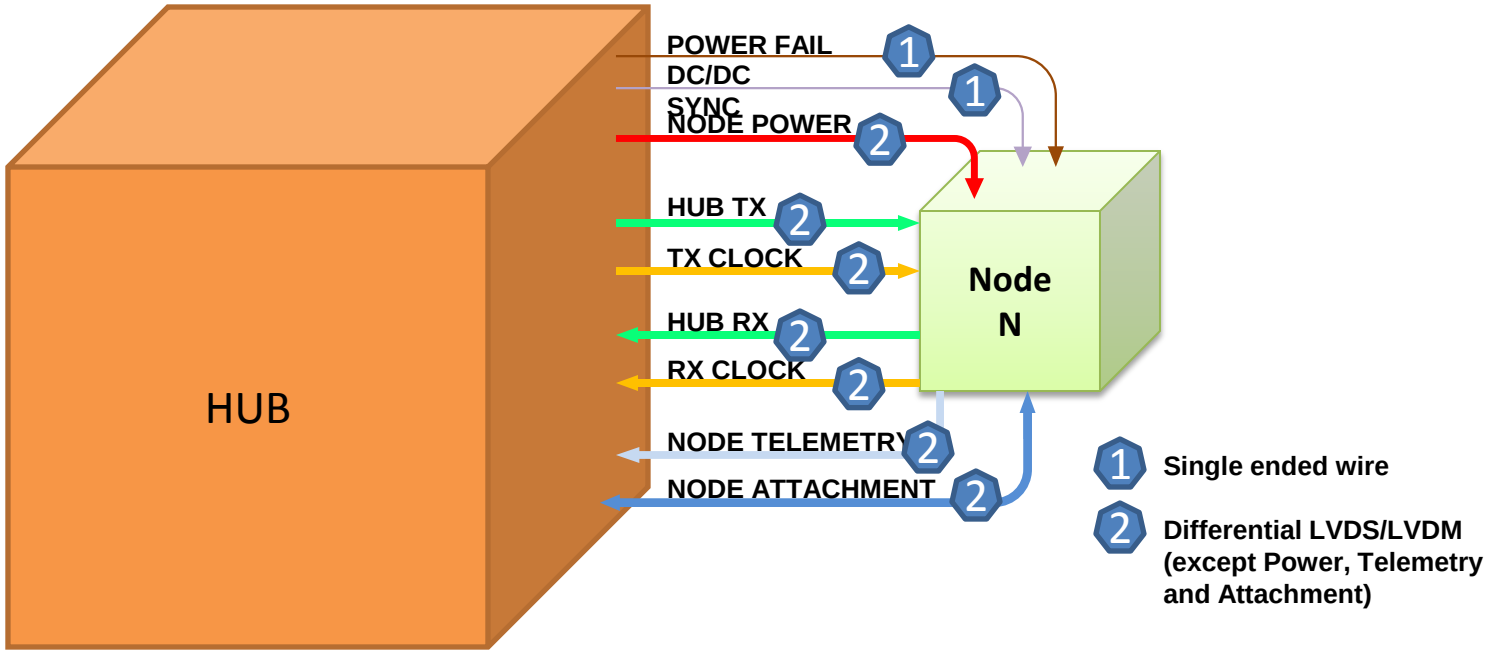
All Nodes communicate with Hub concurrently through full duplex I/F

All connections are done through dedicated, fault isolated, differential I/F
No shared connections !

Proposed SpaceAGE Bus System Functions

- **Data**
  - Serial communications from HUB to each NODE
    - Data rates per link: from 1Kbps to up to 3.125Gbps (user configurable and programmable)
    - Differential pairs for Full duplex operations
    - Multiple streams: HUB can talk simultaneously to more than one NODE
    - HUB-to-HUB talk in redundant system architecture
    - Flexible data transfer protocols such as SpaceWire, SpaceFibre, PCI Express, etc: all can co-exist in 1 system
    - AC coupling for better CMV protection
- **Power**
  - 28V bus switched power distribution from HUB
    - Up to 20-30W RMS power per NODE
    - Electrical isolation between Hub(s) and Nodes
    - True “hot” plugging/unplugging for all NODEs and HUBs without disturbing other system components
    - Capability to work directly with 120V power bus voltages
- **Clock**
  - Individually distributed from HUB to each NODE
    - User programmable clock distribution for S/C events synchronization
    - Single frequency power supplies synchronization
- **Analog telemetry**
  - HUB will process all Node telemetry (with 0.1% accuracy); Node requires to have:
    - Either differential multiplexer and signal scale conditioner for NODE analog signals (0.1% accurate) , or
    - Single thermistor, if any NODE analog circuitry is undesirable
- **Auxiliary**
  - Facilitate NODE control from HUB
    - Independent reset for each module
    - Single frequency power synchronization
    - Allow true hot plugging/unplugging of each module

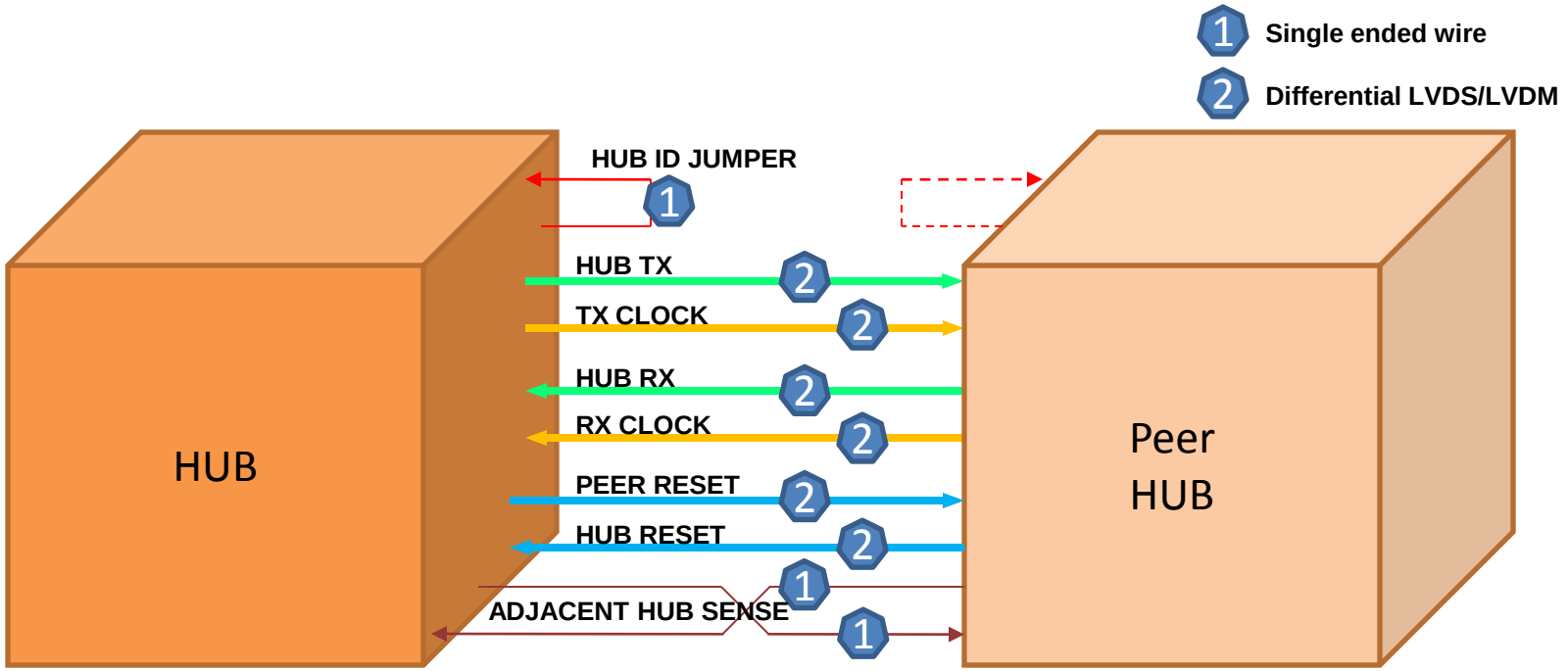
HUB to NODE Connections



Only 16 wires per NODE are needed to transfer all essential bus functions

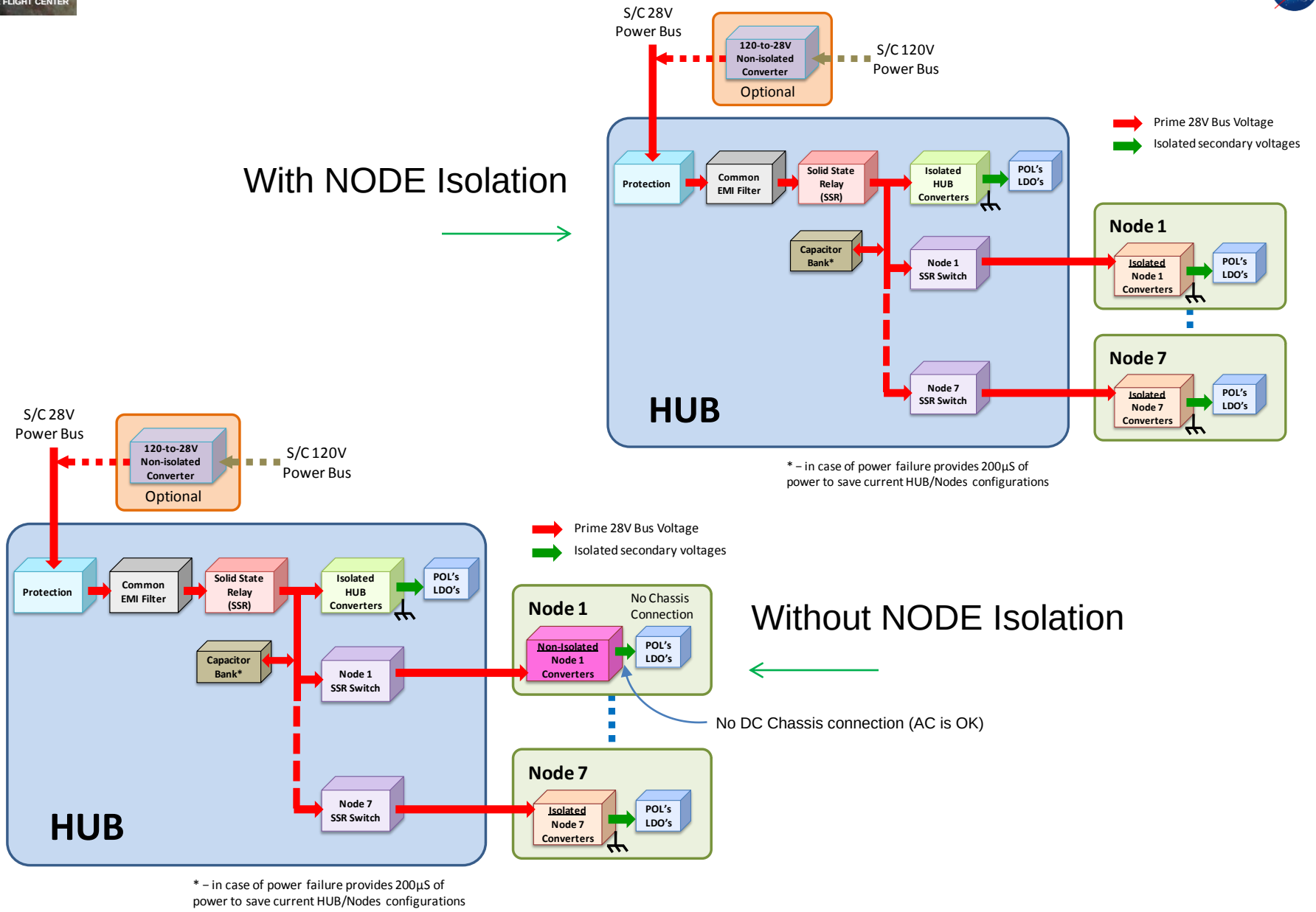
If redundancy is required – NODE will get the same wire set from peer HUB

HUB to HUB Connections



Only 16 wires per HUB are needed to exchange with all essential functions

SpaceAGE Bus Power Distribution



Proposed SpaceAGE Bus System Summary

- **Ease of implementation**
  - Simple electrical interface
    - Only 16 physical copper wires per link which are capable to satisfy requirements for 90% or more missions
  - Simple mechanical interface
    - Only connectors position is defined
    - No restrictions for module width
- **Much easier compatibility between various vendors**
  - No custom user functions for standardized back connectors
- **Increased data throughput on subsystem level**
  - Serial links will provide higher data rates
  - Double processing/communication rate when 2 HUB modules are plugged in
- **User expandability**
  - Front and Top surfaces are reserved for User connectors
  - Multiple cards per module
- **Lower mass and volume over parallel bus design**
- **Superior heat transfer**
  - Elimination of wedge locks: direct contact between cards and module's frame
  - Larger contact surfaces between module body and chassis
- **EMI/EMC issues**
  - 100% EMI shielded
  - Lower emitted noise due to a possible total synchronization of all units
- **System reliability**
  - Single string, or
  - Dual independent redundancy, or
  - System cross-redundancy
- **Wide range of applications**
  - Can be used for human or robotic missions

Connector's Desired Requirements

- **Minimum number of conductors**
  - 16, with capability of expansion
- **Wires**
  - Up to AWG#24 wires for power transfer
- **Impedance matching**
  - 100 ohms differential
- **High speed performance**
  - Up to 4 Gbps
- **Shielding**
  - Fully EMI shielded
- **Connectivity**
  - Blind mateable
  - Scoop proofed
- **Material**
  - No vacuum outgassing and weightlessness wiskering
- **Shape**
  - Rectangular for small real estate use

Suggested Connector Type

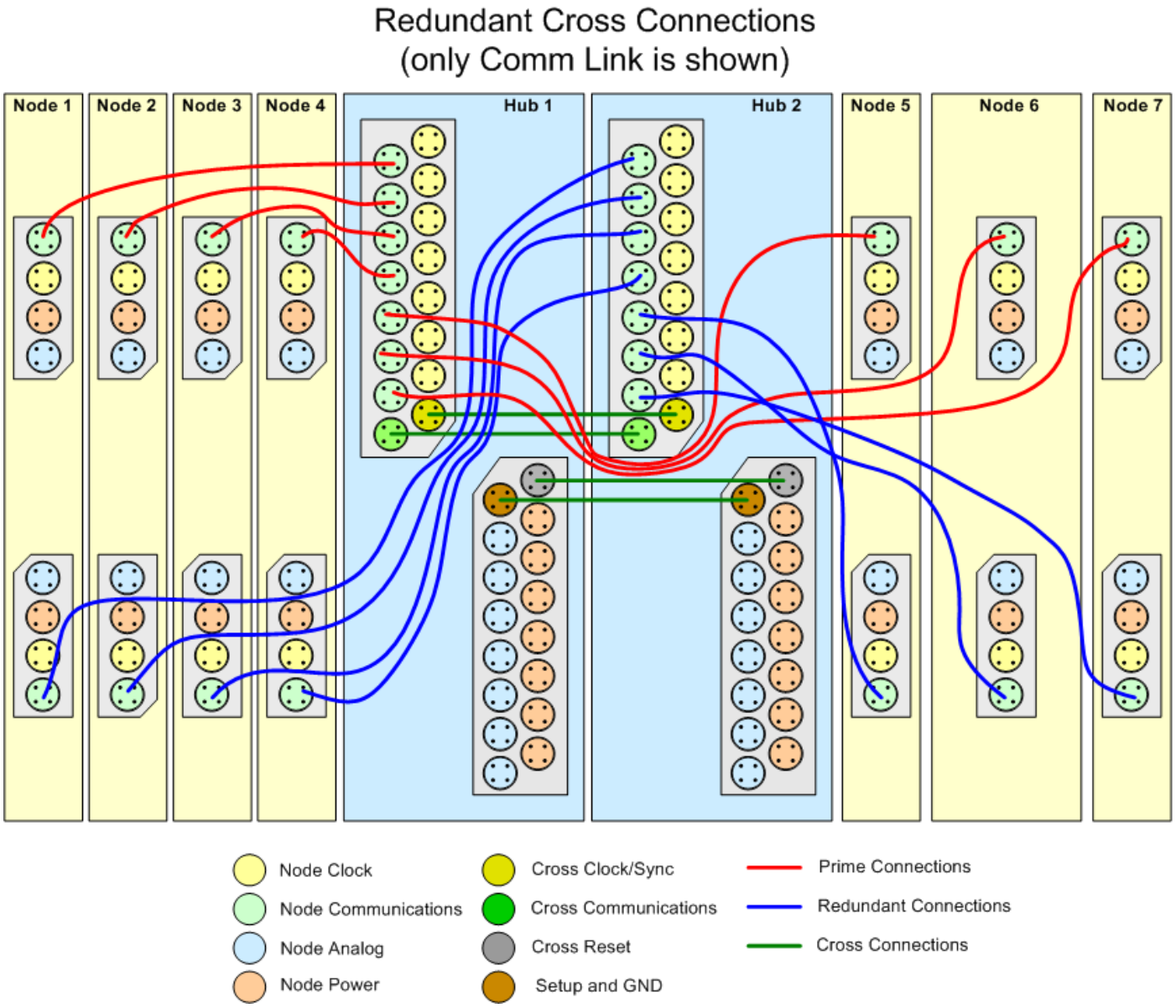
Rugged D-Sub miniature from Sabritec Inc. with Quadraxial pin assembly inserts

4 (shown) and 16 position shells are suggested

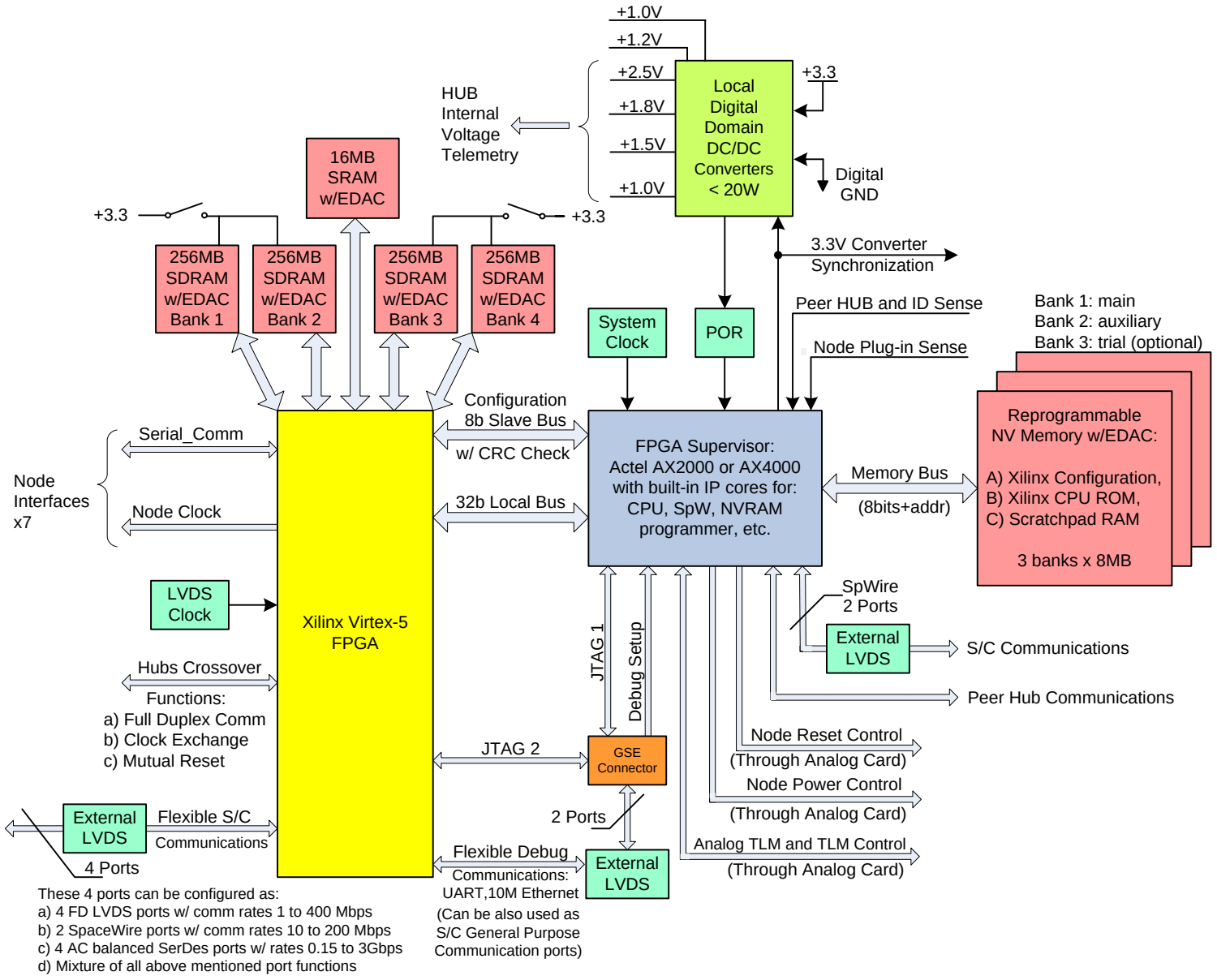
Proposed Signal Assignments

Group	Sub Group	Function	Pin	Node Bus Connector	Flow Direction	Hub "A" Bus Connector	Flow Direction	Redundant Hub "B"	Notes
Hub to Node Bus (28 inserts out of 32 for 7 Nodes)	Digital	Serial Communication	1	RX+	←	TX+			Full Duplex link. Diagonal pins 1-3 and 2-4 provide 100Ω impedance
			2	TX+	→	RX+			
			3	RX−	←	TX−			
			4	TX−	→	RX−			
		Clock and Reset Distribution	1	Clock_in+	←	Clock_out+			Clock function is defined by Node end user Node can be reset individually by Hub
			2	Reset_in+	←	Reset_out+			
			3	Clock_in−	←	Clock_out−			
			4	Reset_in−	←	Reset_out−			
	Power and Analog	Power and Supply Sync	1	Node **Power**	←	Node Power			Up to 1.5A@28V of derated Node current; DC/DC Sync is 200-800KHZ free running 5V clock; Hub generated Power Fail
			2	**Power** Return	←	Power Return			
			3	DC/DC_Sync_in	←	DC/DC_Sync_out			
			4	Power Fail	←	Power Fail			
		Analog Telemetry and Node Sense	1	Analog_out+	→	Analog_in+			Each Node may have 4-16 analog telemetry slots or just 1 passive thermsitor; "Sense" tells Hub if Node is plugged in and secured
			2	Analog_out−	→	Analog_in−			
			3	Sense_out+	→	Sense_in+			
			4	Sense_out−	→	Sense_in−			
Hub to Hub Crossover Bus (4 inserts for an extra Hub)	Digital	Cross Communication	1			X_TX+		X_TX+	Full Duplex cross link. Diagonal pins 1-3 and 2-4 provide 100Ω impedance
			2			X_Clock_out+		X_Clock_out+	
			3			X_TX−		X_TX−	
			4			X_Clock_out-		X_Clock_out-	
		Cross Clock	1			X_RX+		X_RX+	Allows both Hubs to share common clock
			2			X_Clock_in+		X_Clock_in+	
			3			X_RX−		X_RX−	
			4			X_Clock_in-		X_Clock_in-	
	Reset and Config	Cross Reset	1			X_Reset_out+		X_Reset_out+	X_Reset allows each Hub to reset its peer Hub either by command, or by lack of communications for the TBD time period
			2			Peer_Hub out		Peer_Hub out	
			3			X_Reset_out−		X_Reset_out−	
			4			Config_out	X	Config_out	
		Master-Slave Configuration and Peer Hub Plug-in	1			X_Reset_in+		X_Reset_in+	Peer_Hub tells each Hub that its Peer Hub is in
			2			Case GND		Case GND	
			3			X_Reset_in−		X_Reset_in−	Master Hub (A) - no jumper, Slave (B) - external jumper
			4			Case GND	X	Case GND	

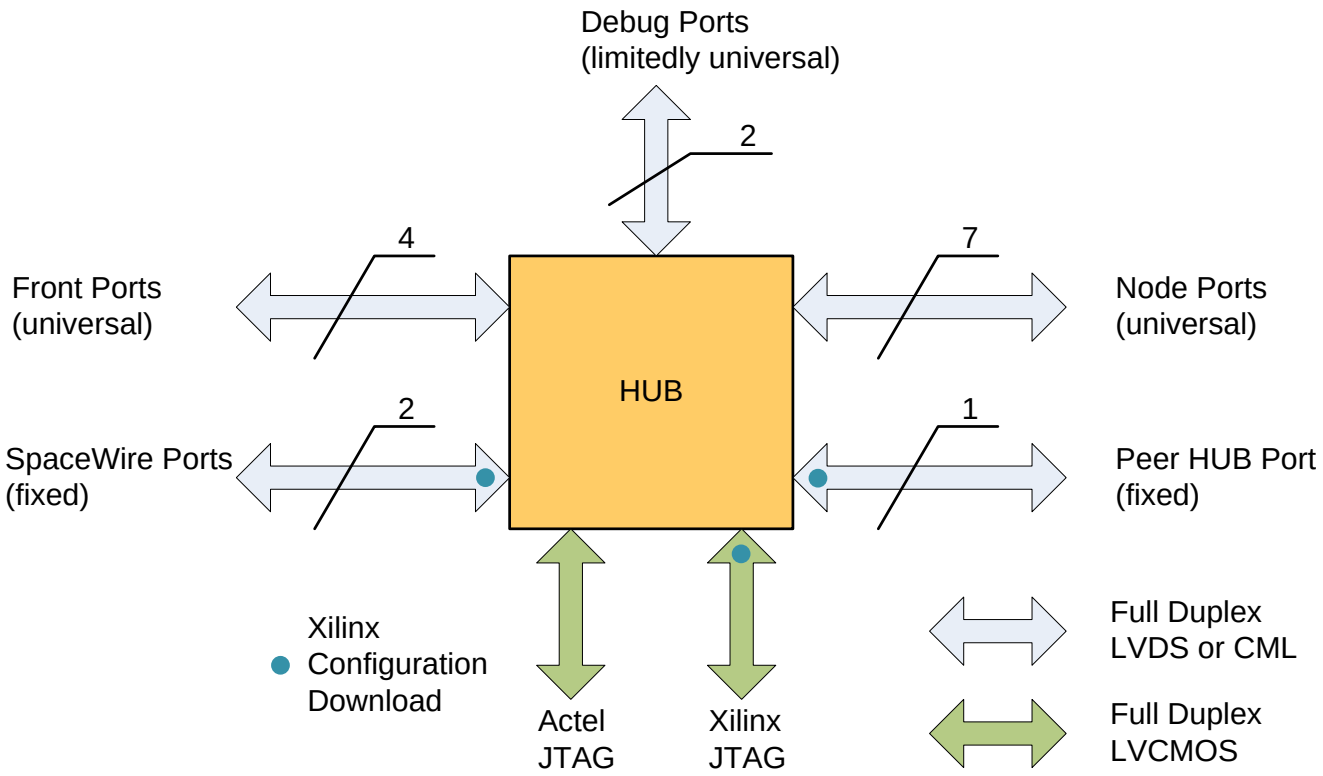
One of Proposed Routings



Suggested HUB Architecture (Digital Section)



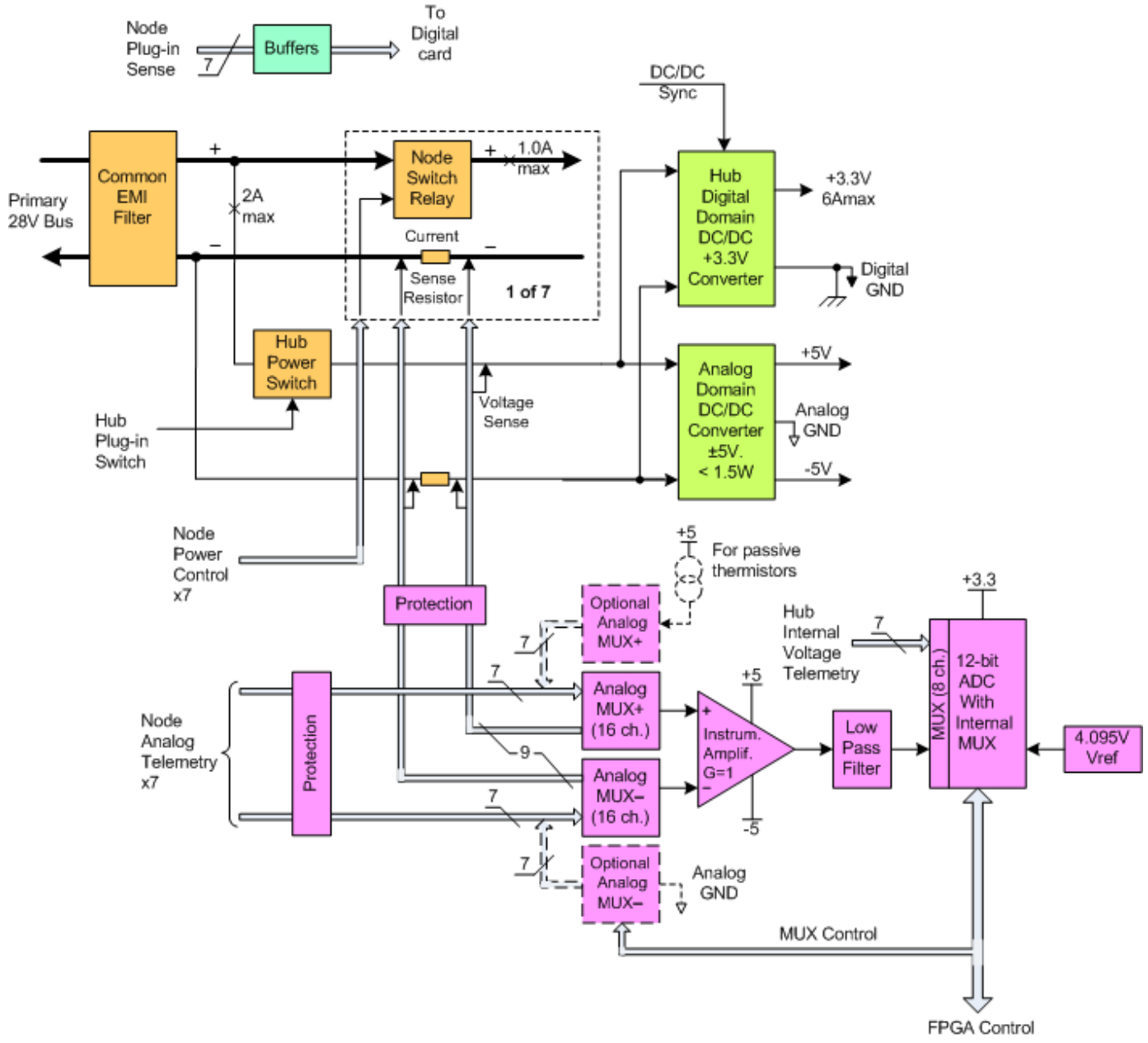
Suggested HUB's Communication Ports



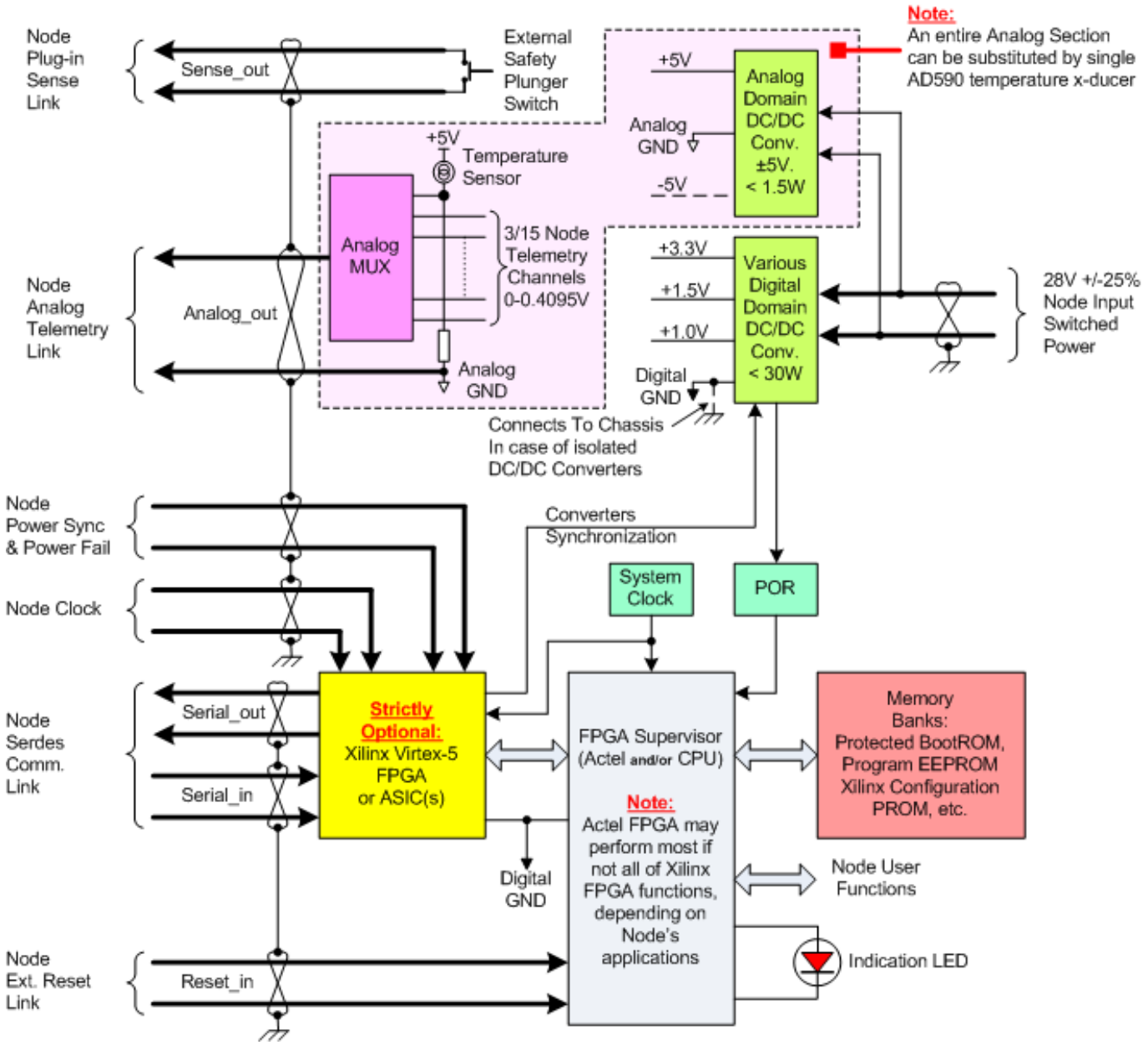
Suggested HUB's Ports Highlights

	Back (SpaceAGE Bus Ports)	Front (S/C Ports)	Top (mostly for debug)
Number of ports	**8**: **7** NODE(Universal) + **1** Peer HUB	**6**: **4** Universal + **2** SpaceWire	**2**: Limited Universal
Physical Interface	Buffered LVDS or AC coupled CML SerDes		Buffered LVDS
Duplex	Full	Full	Full
Speed range	1Kbps to 3.125Gbps (up to 100Mbps for SpW)		10Kbps to 100Mbps
Additional Sync clock	Yes	No	No
Protocols	Any type sync or async	Any async + SpW	Async + 10M Ethernet
In-flight re-configuration	Yes (except Peer HUB)	Yes (except SpW)	Yes (if used for flight)
State when not used	Hi-Z	Hi-Z	Hi-Z
Multidrop network use	No	Possible (to 400Mbps)	No

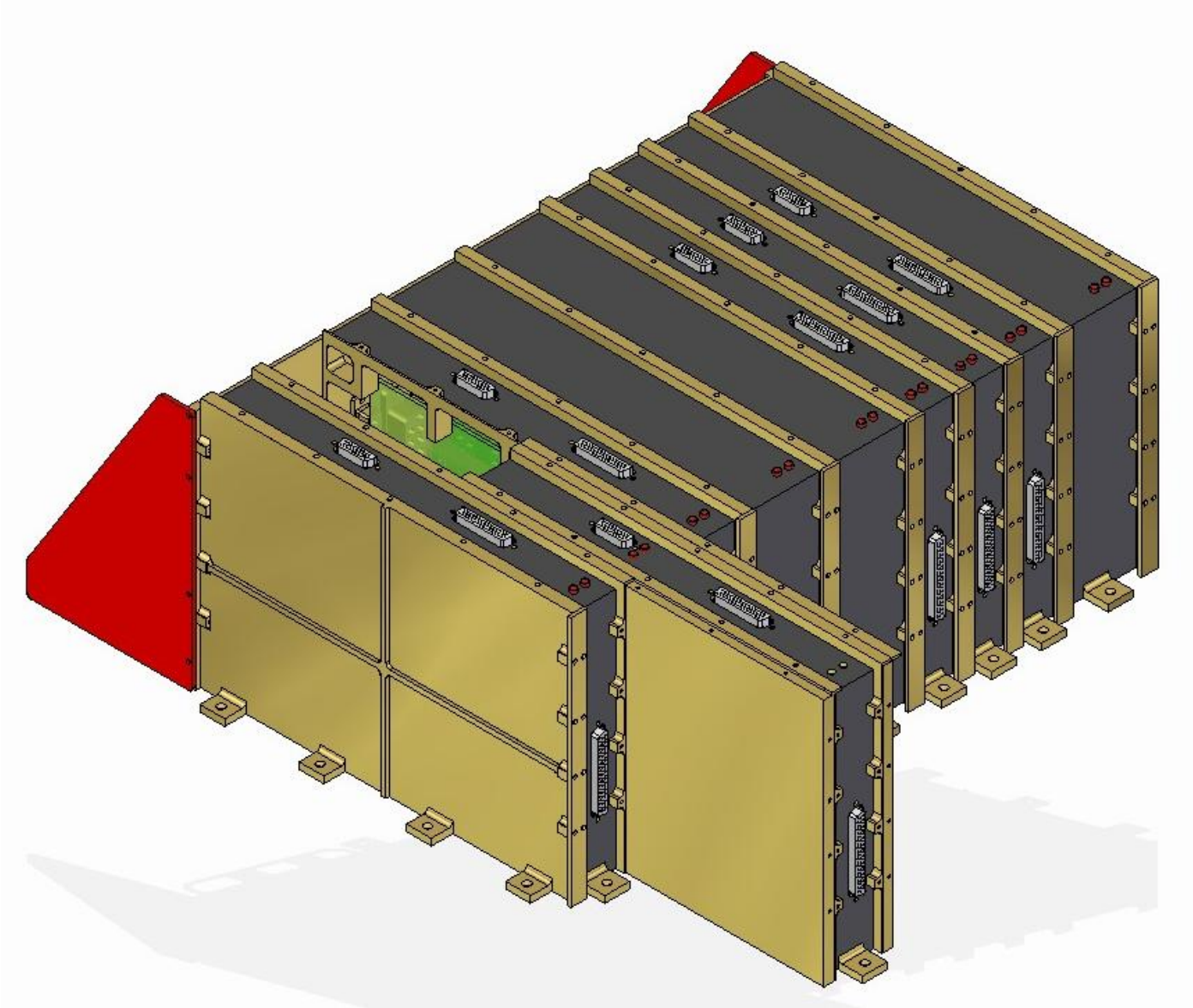
Suggested HUB Architecture (Analog TLM & Power Section)



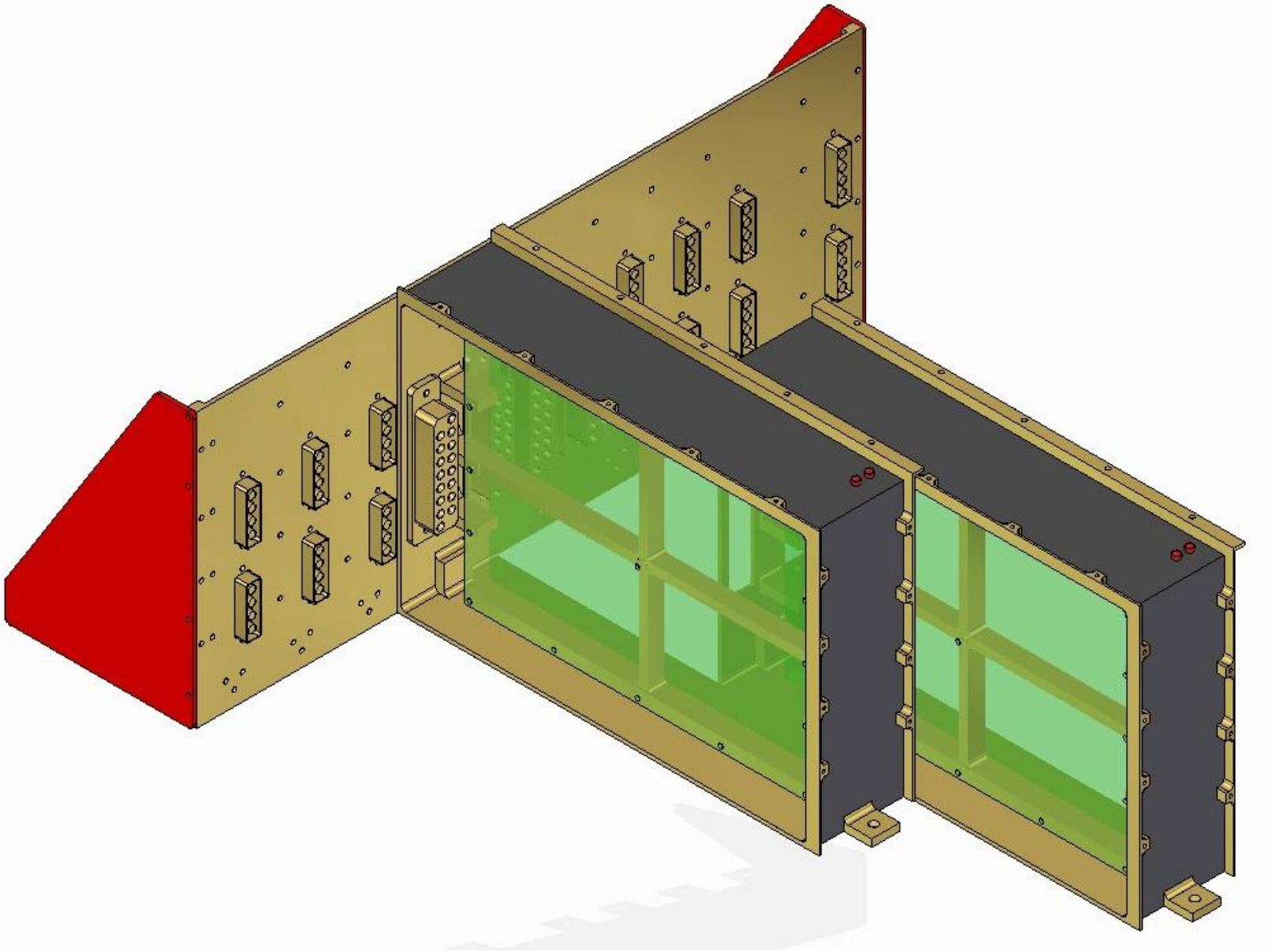
Suggested NODE Architecture



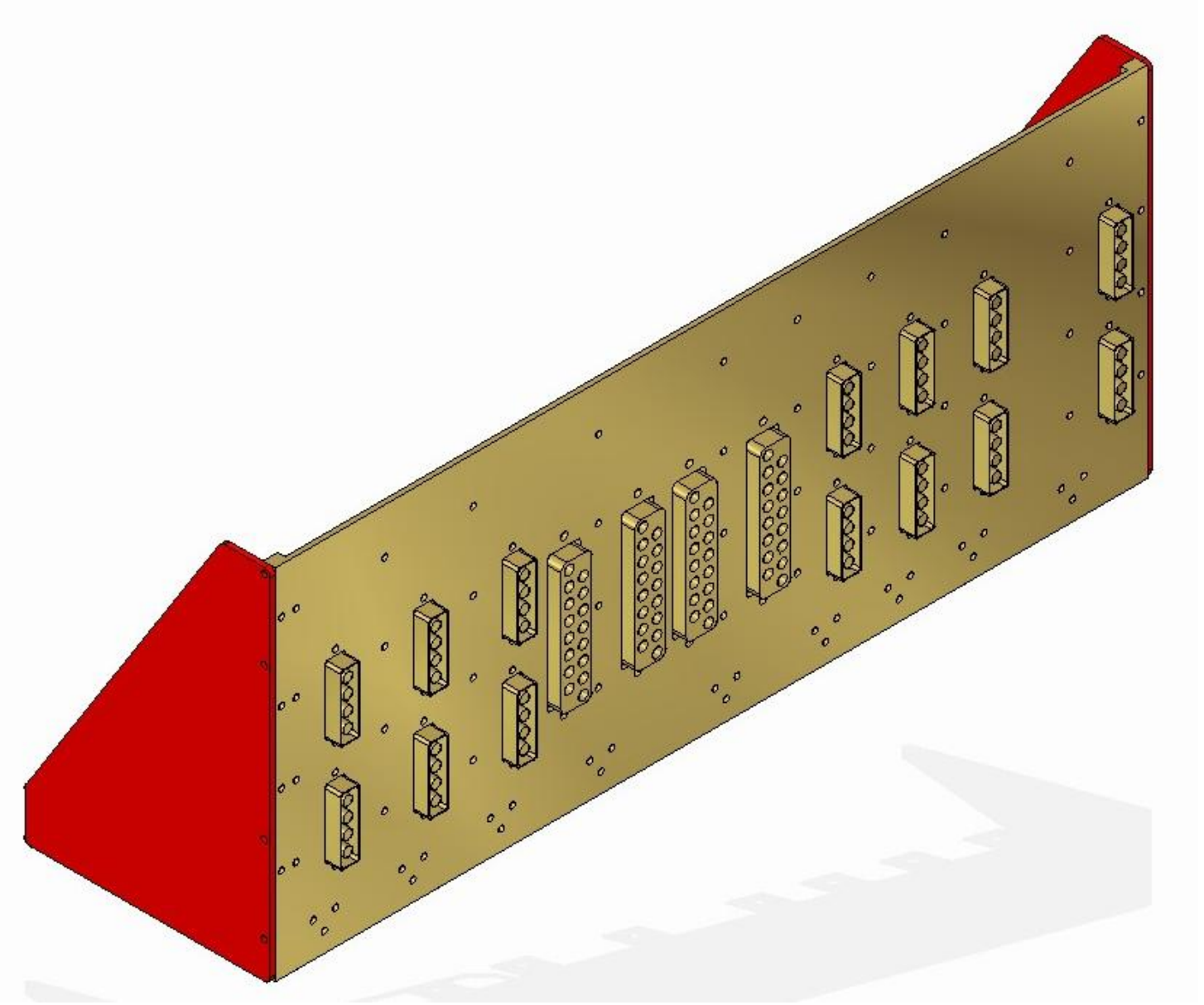
Assembled System View



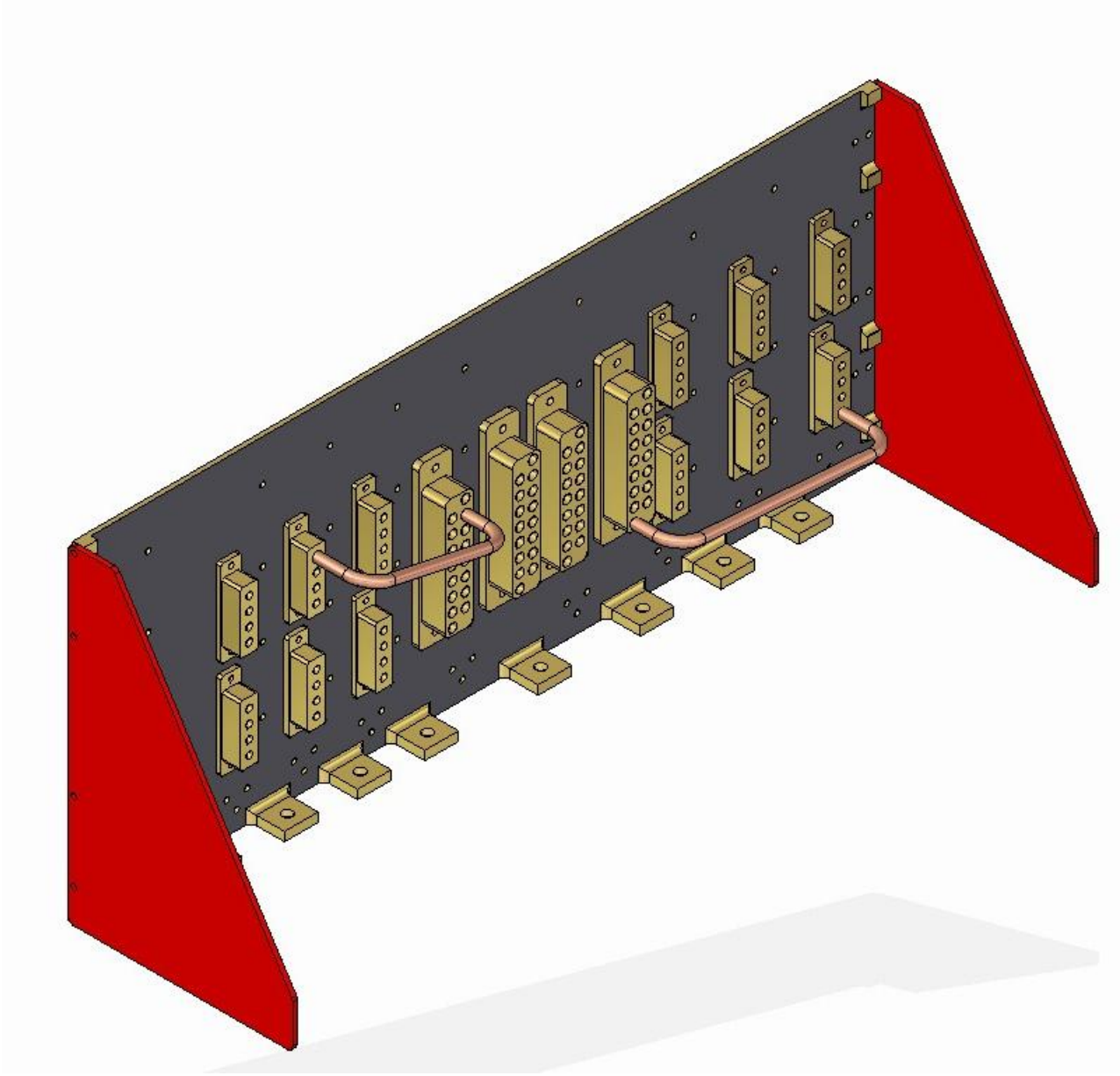
Transparent View



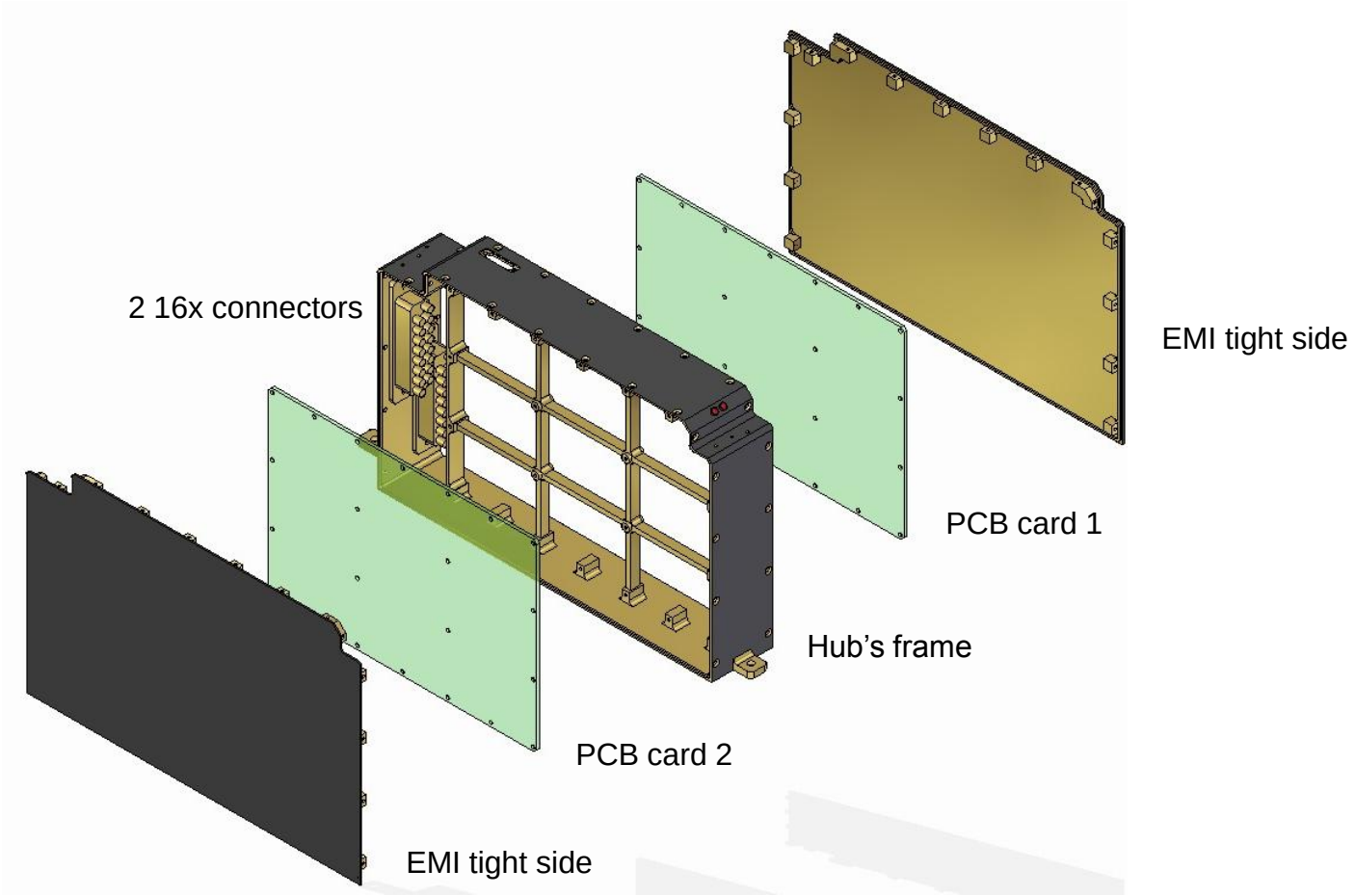
L-Bracket Front



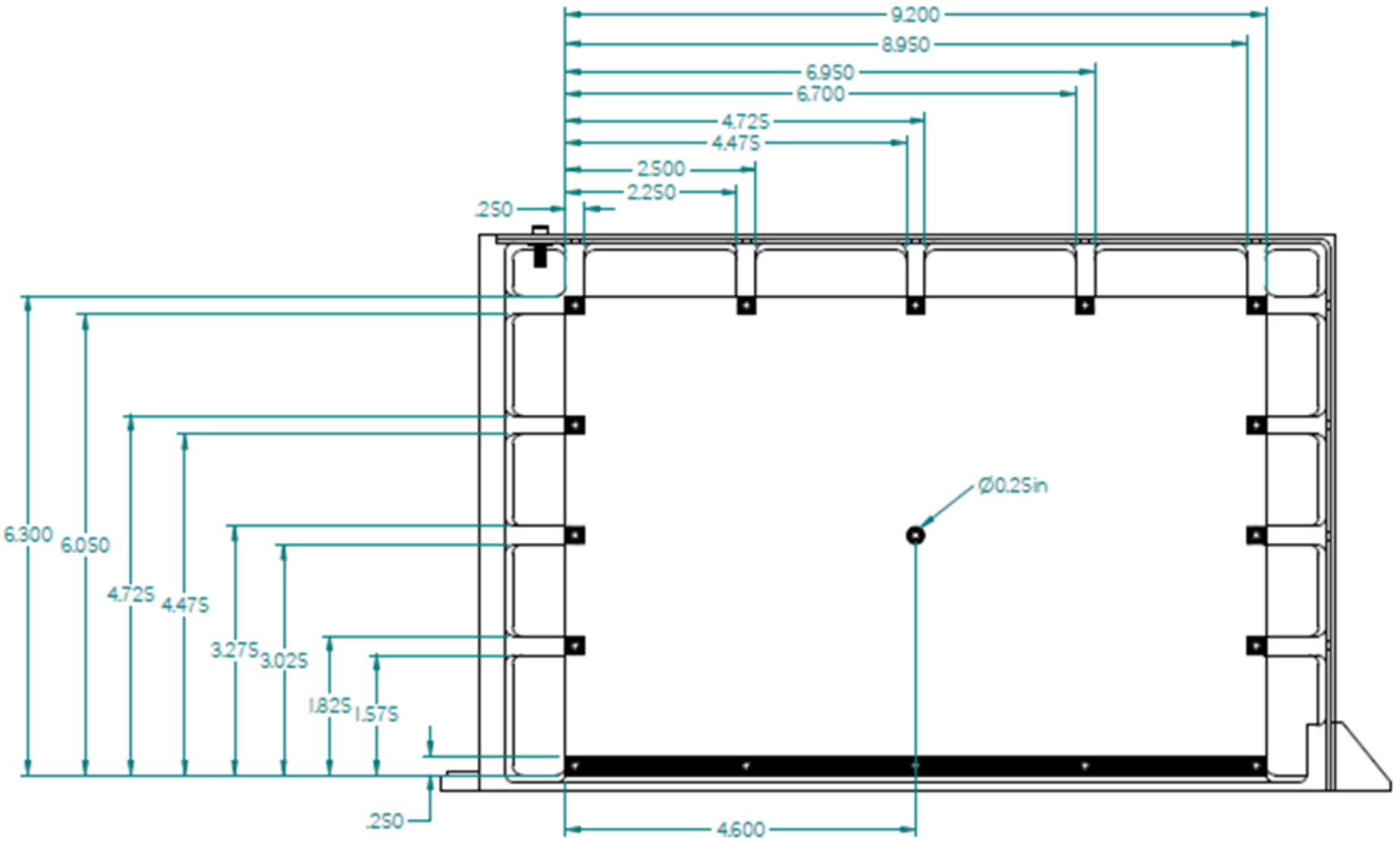
L-Bracket Back



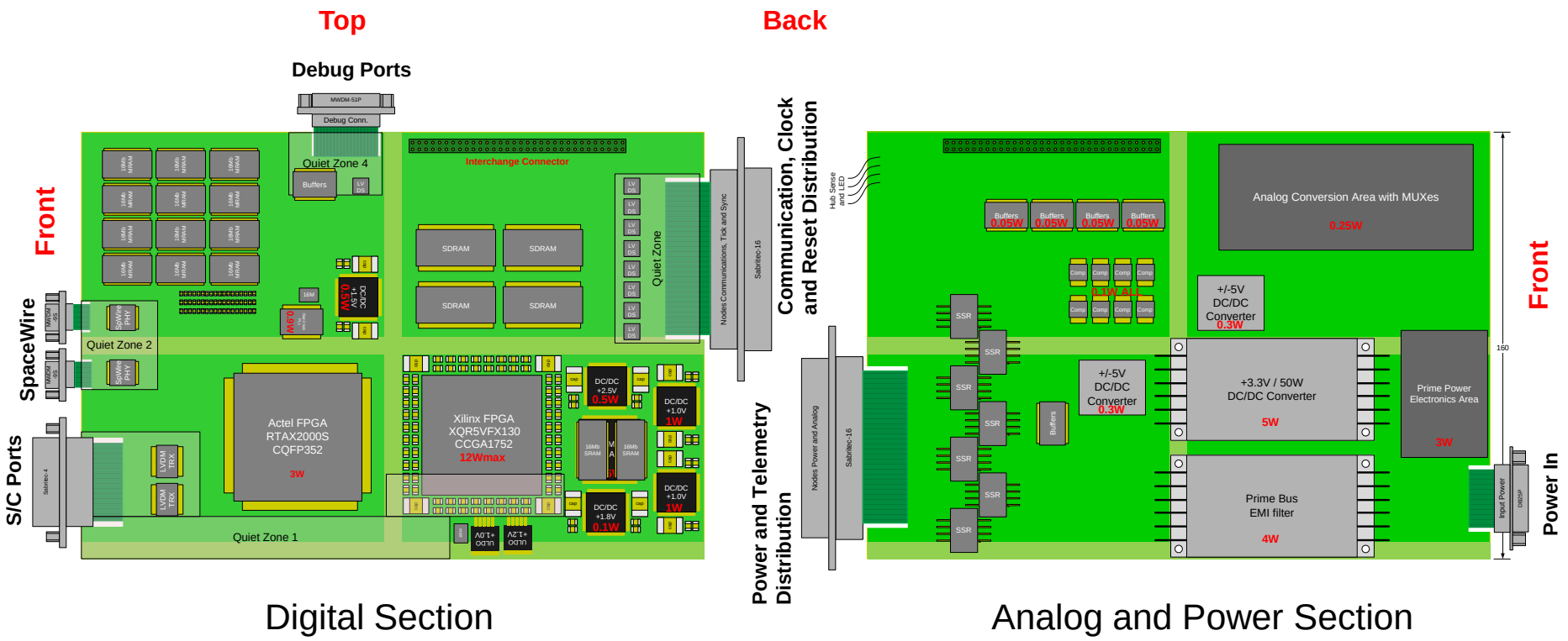
Suggested Dual Cards Assembly for HUB Module



Suggested Cross Section View for HUB Enclosure



Suggested Layouts for HUB



Overall Buses Comparison Chart

Function	Traditional Buses	Suggested SpaceAGE Bus
Data Interface	Parallel	Serial
Data Exchange	Half-duplex	Full-duplex
Data Exchange Method	Synchronous	Asynchronous
Impedance Matching	Mismatched	Matched
Bus Utilization	Single flow	Multiple independent flows
Redundancy	Single	Single, Double, Cross
Power Distribution	Multiple bus voltages	Single voltage
Bus Current	Medium to very high	Low to very low
Common Voltage Tolerance	Low (100's of mV)	High (several volts)
Card-to-Card Isolation	Very complex/Impossible	Possible and very simple
Hot Plugging/Unplugging	Complex/Impossible	Possible and very simple
System Telemetry	Not Specified	Standard: Analog & Digital
EM Interference	Leaking	Fully shielded
Clock Distribution	Single high frequency	Multiple user defined frequencies
Clock Skew Requirements	Very tight	Low: not very important
Connector Pins per Card	Several hundreds	16 per Node plus Chassis
Bus Interconnect	PCB	Harness
User Connectors Areas	Front surface only	Front and top surfaces
PCB Assembly	Single side w/limited back	Dual sided, w/unlimited tier cards
Card Insertion Force	Medium to high	Low
Blind Mating	Yes, stress on conn. pins	Yes, stress on conn. metal body
Scoop Proofing	Yes	Yes
Cards or Modules Distance	20-25mm	Limited by communication rates

The End

Questions?