BAE SYSTEMS

Leveraging SpaceWire Network Prototyping to Create Flexible SpaceWire Components and Support Software

International SpaceWire Conference 2011

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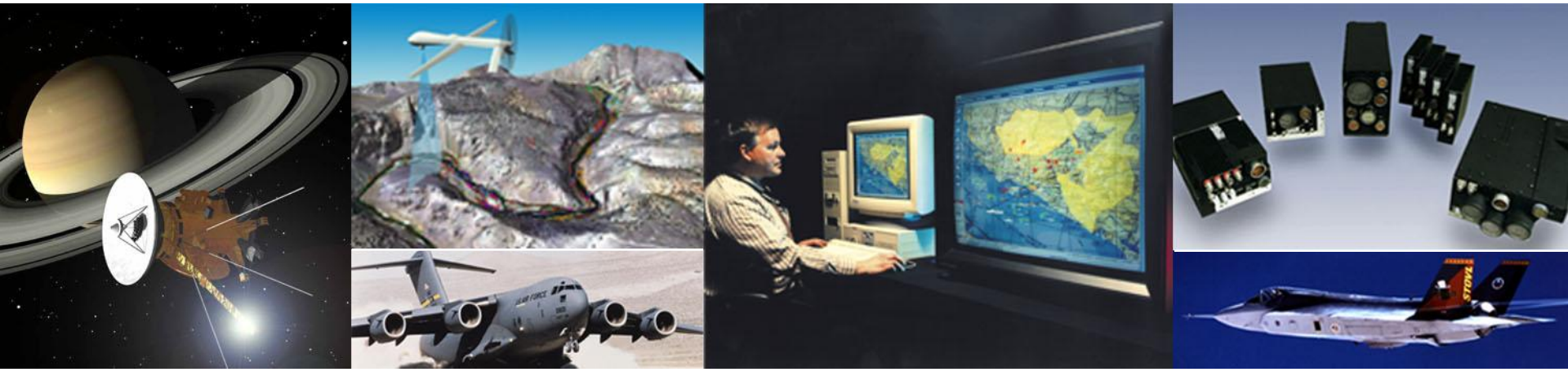

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Agenda

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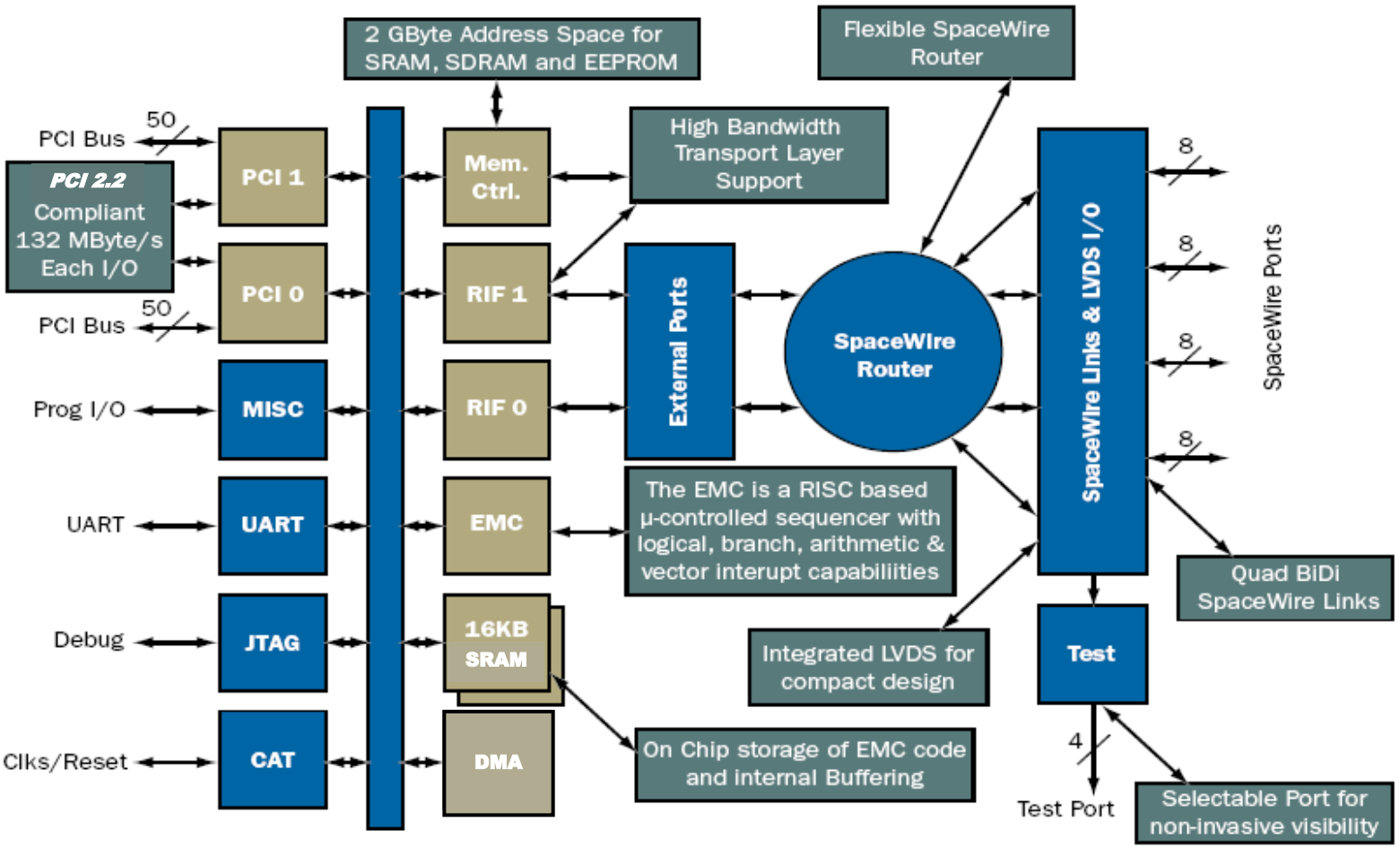
- Topologies and Node Types
- Demonstration Approach and Topology
- Demonstration Node Designs
- SpaceWire Endpoint ASIC with Embedded Microcontroller
- Node Improvements including RMAP
- SpaceWire Middleware
- SpaceWire Test and Debug
- Summary

4 Port SpaceWire TRL 9 ASIC Block Diagram



Core-based SOC Heritage

Potential SpaceWire Network Topologies

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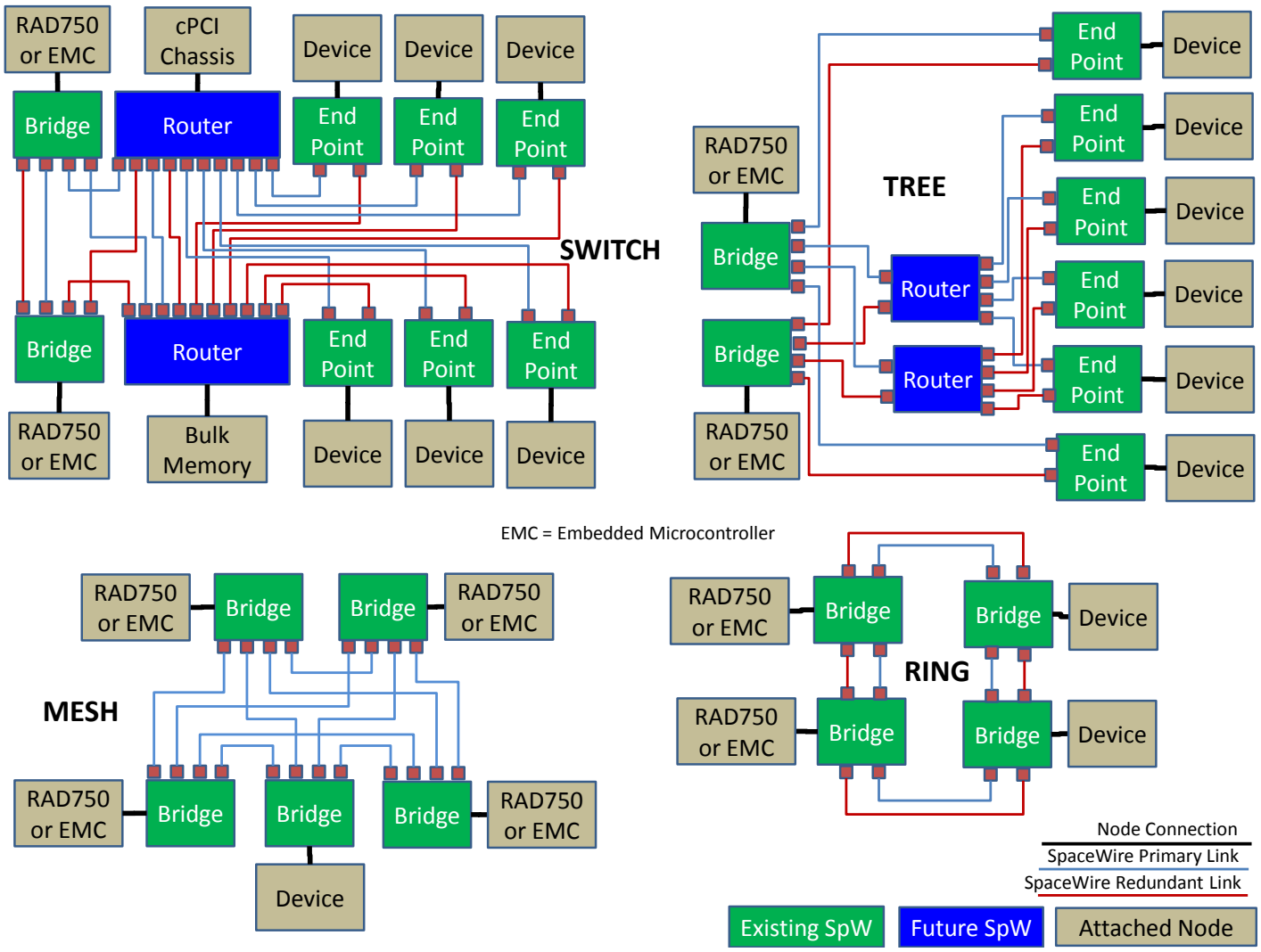

Three network devices types efficiently create any network topology

Topology Effects on Network Attributes

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	Ring Network	Tree Network	Switch Network	Mesh Network
Topology	General purpose; dual path to each node	Large number of devices under control of small number of nodes - 1553 replacement; longer	backplane or localized network; common assets may be shared	many peers all sharing or sending and receiving data; localized
Nodes using only 1-2 port endpoints	Expandable Ring - must have 2 port router	can only be leaves of tree	can only be nodes connected to switch	two hosts with one port; up to three hosts with two ports
Nodes using only 4 port routers	Two expandable Redundant Rings: 2 ports each	Each Node supports up to three branches	up to four port switches; then must daisy chain (2x4=6; 3x4=9, etc.)	up to five hosts
Nodes using only 6 port routers	Three expandable Redundant Rings: 2 ports each	Each Node supports up to five branches or dual sets of two branches	up to six port switches; then must daisy chain (2x6=8 or 10; 3x6=12or15)	up to seven hosts
Nodes using only 8 port routers	Four expandable redundant rings: 2 ports each	Each node supports up to seven branches or dual sets of three branches	up to eight port switches; then must daisy chain (2x8=12 to 16; 3x8 = 15to24)	up to nine hosts
Nodes using only 12 port routers	Six expandable redundant rings: 2 ports each	Each node supports up to eleven branches or dual sets of five branches	up to twelve port switches or dual six port switches; then must daisy chain (2x12=18to22)	up to thirteen hosts
Nodes using only 16 port routers	Eight expandable redundant rings: 2 ports each	Each node supports up to fifteen branches or dual sets of seven branches	up to sixteen port switches or dual eight port switches; then must daisy chain (2x16=20to30)	up to seventeen hosts
Optimal Network Implementation	Two port routers for single ring; Four port routers for redundant rings	Use different sized routers to match localized groups of nodes	Smallest number of largest switch covering number of nodes to get most crossbar effect; if more than one; multiple cross links	Switch sized or used to match number of hosts

Investigated number of router nodes vs. different topologies - Actual topologies may be hybrid requiring endpoints, routers and switches

SpaceWire Demonstration Lab Objectives

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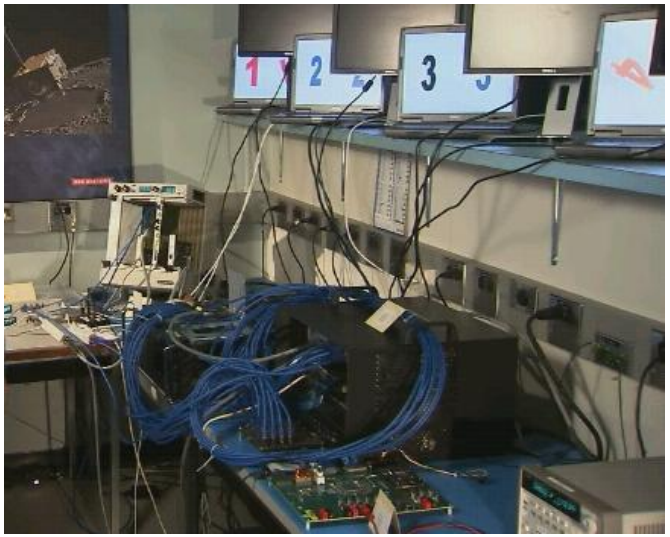
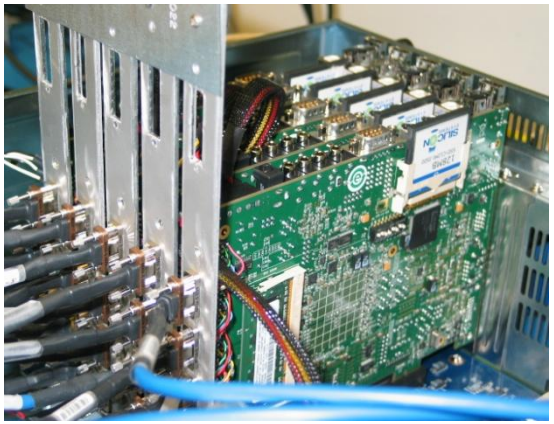
- **Medium bandwidth scalable fabric for space processor systems**
- **Multiple topologies constructed to enable any space application and topology**
- **New capabilities, reusable cores and flight-level ASIC designs prototyped on FPGA boards**
- **Complimentary components to the RAD750 processors with device support and network middleware.**
- **Network discovery, diagnostic and management software testbed**
- **Ability to connect / validate / prototype in-house and customer network applications.**
- **Groundwork for expansion into future fabrics**
  - **SERDES level - Serial RapidIO, SpaceFibre, or…**



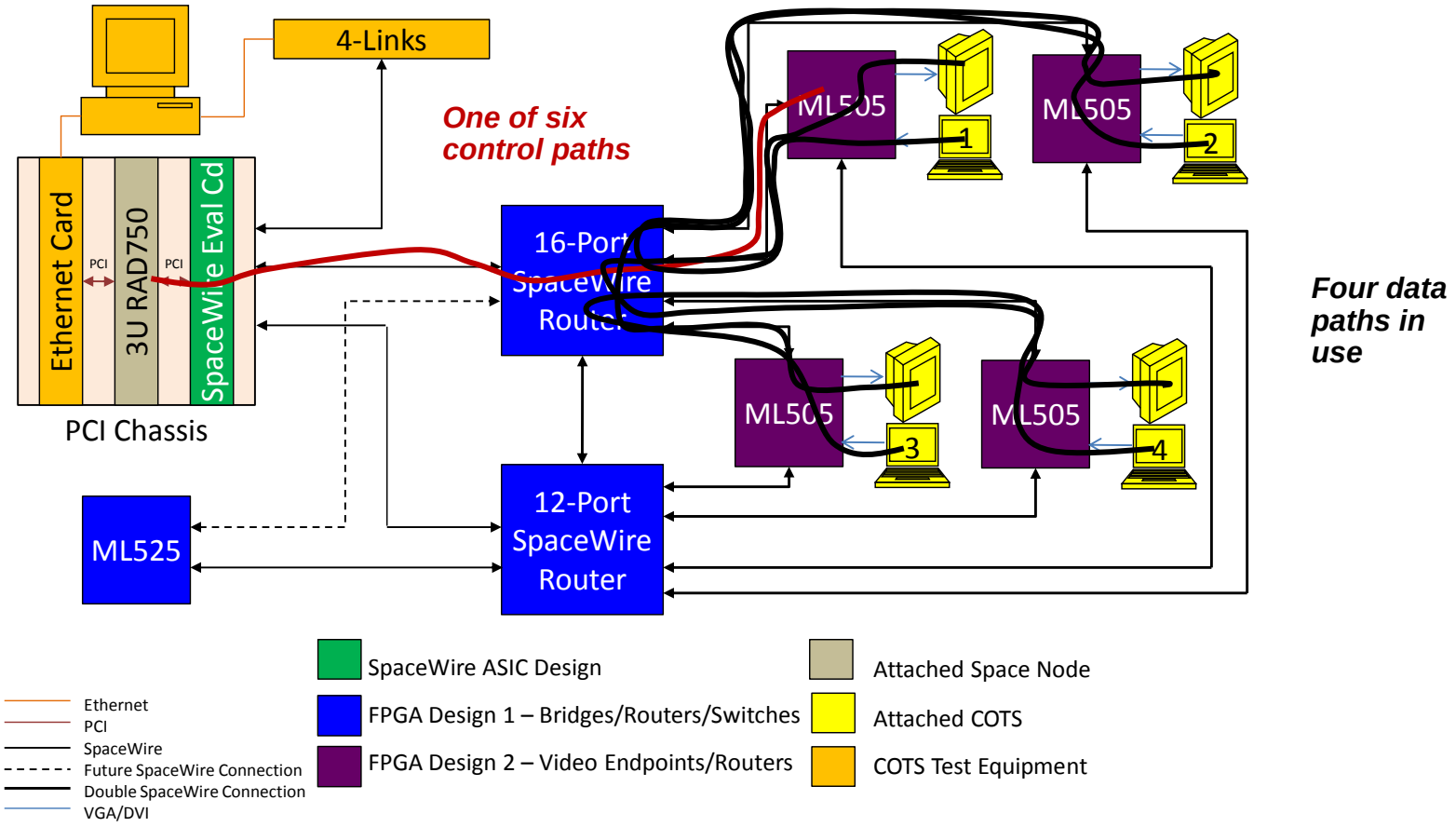


We are continuing to expand demonstration laboratory for both internal development and customer interaction and applications

Demo Dataflow – Chained Video

The dataflow transmits each endpoint's laptop video to another endpoint's monitor. It uses two SpaceWire links for each video stream

Just one of many possible application mappings



FPGA Design 1:

4 Port Bridge to 16 Port Router/Switch

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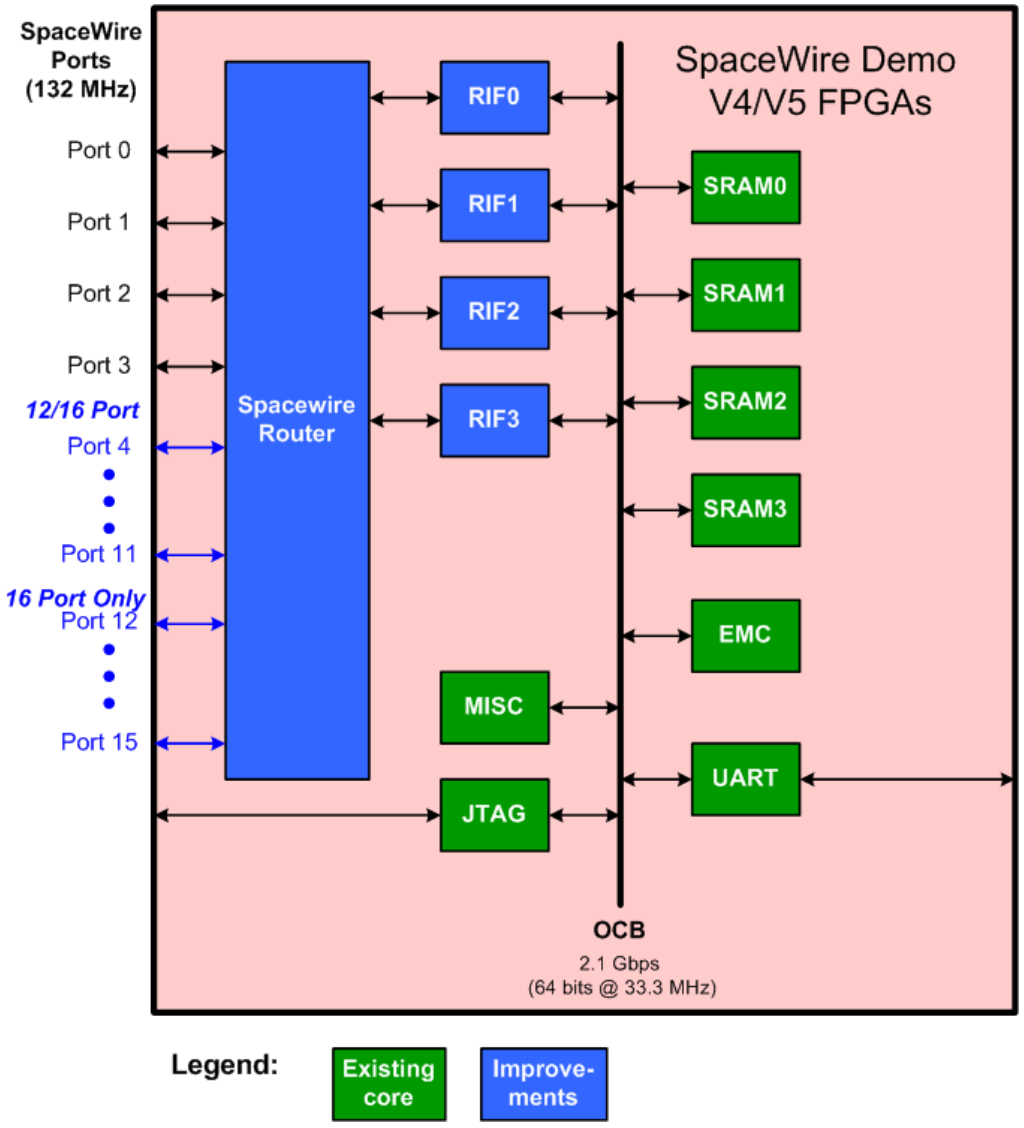
- **This design is used in the 4-Port Bridge, 12-Port and 16-Port Router /Switch FPGAs.**
- **The only difference between the implementations is the additional external SpaceWire Ports. (The number of LVDS pairs wired on a COTS board was the limiting factor in the number of SpaceWire ports for each board).**

Full SpaceWire Routers with EMC



FPGA Design 2:

4 Port Video Source/Sink Endpoints

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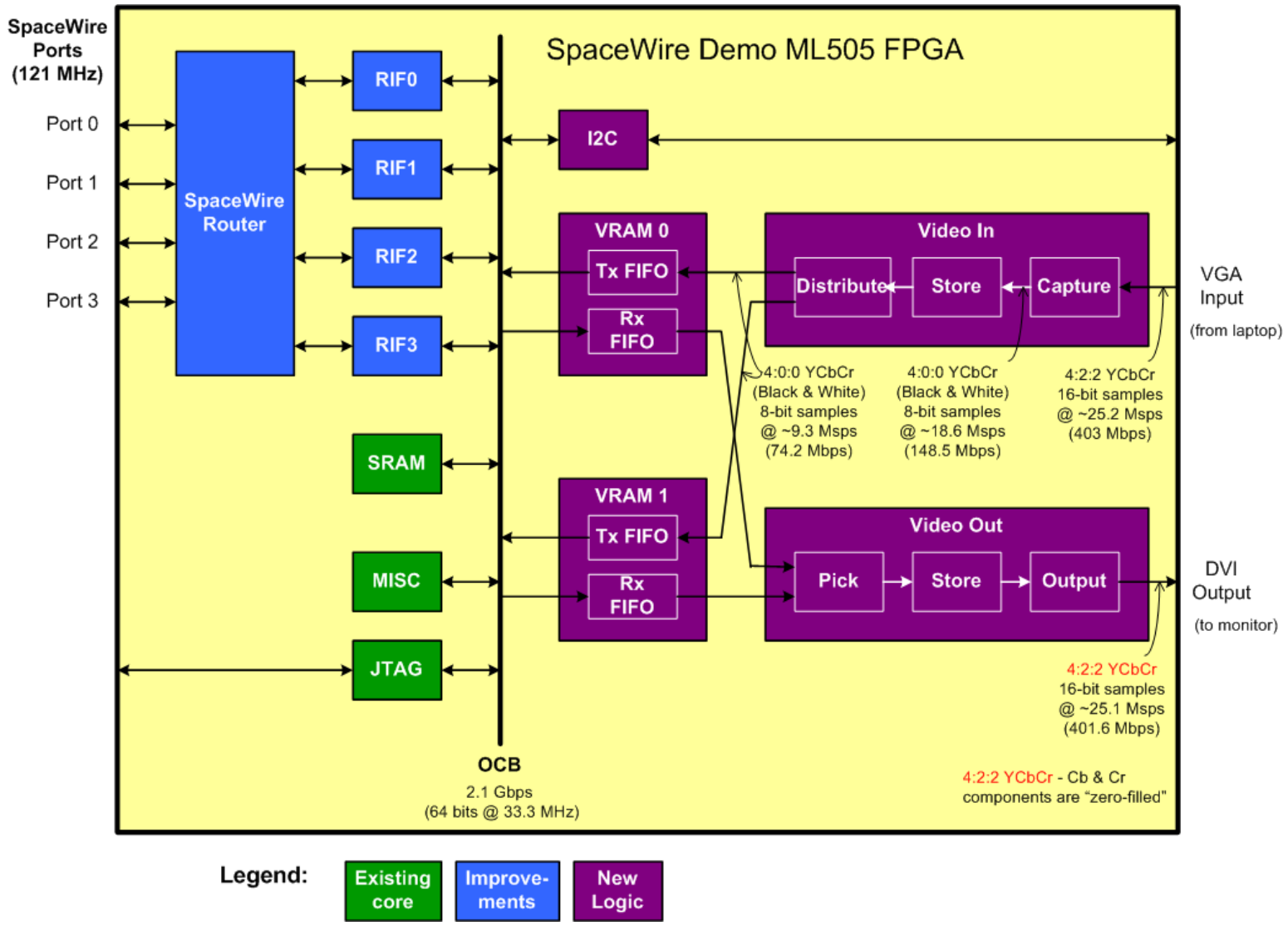
Endpoint Data Sync And Source



SpaceWire Endpoint ASIC FPGA Prototype

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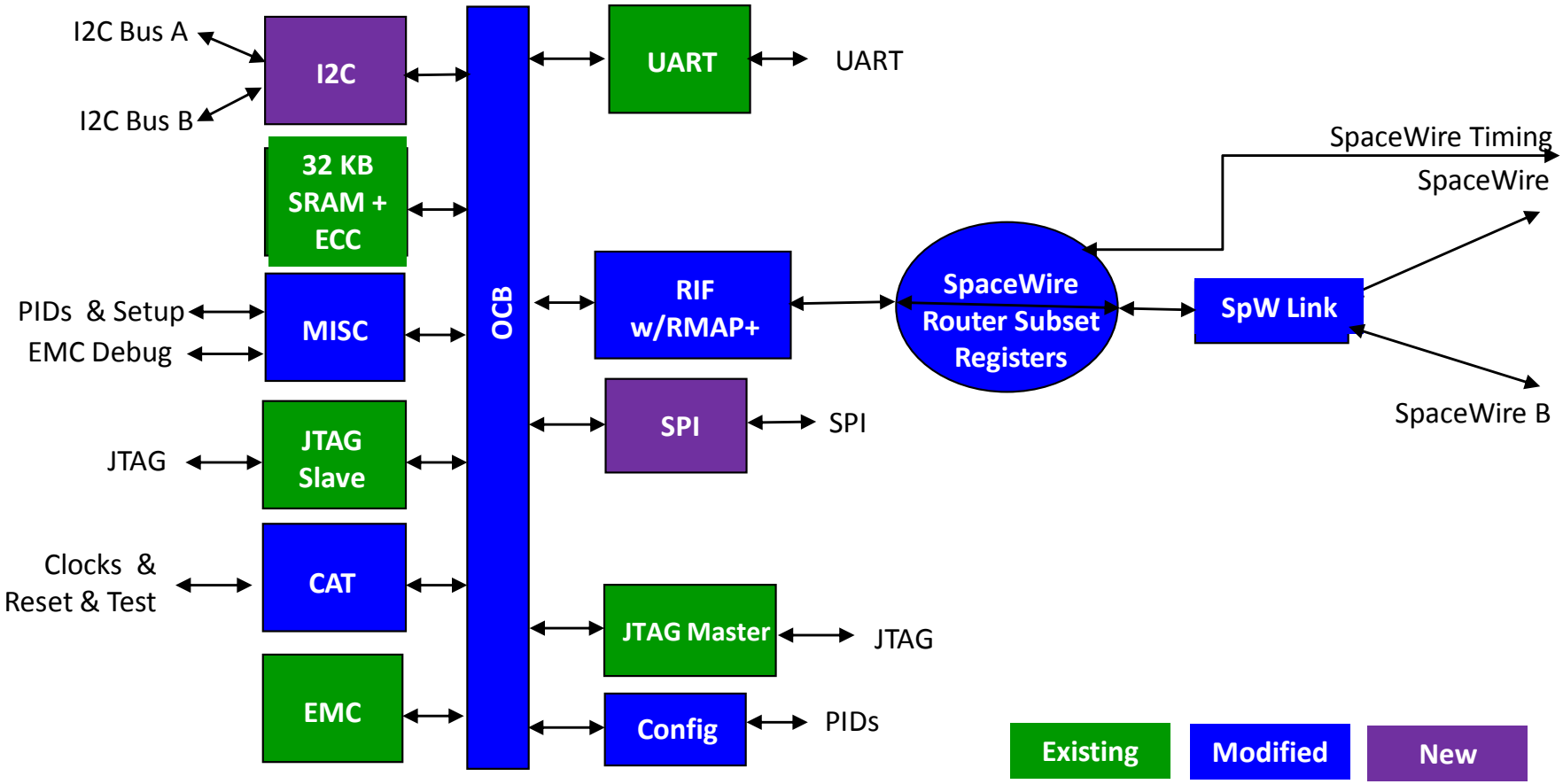

Utilizing Demonstration Lab to Debug future ASIC using same cores as in demonstration

SpaceWire Endpoint ASIC

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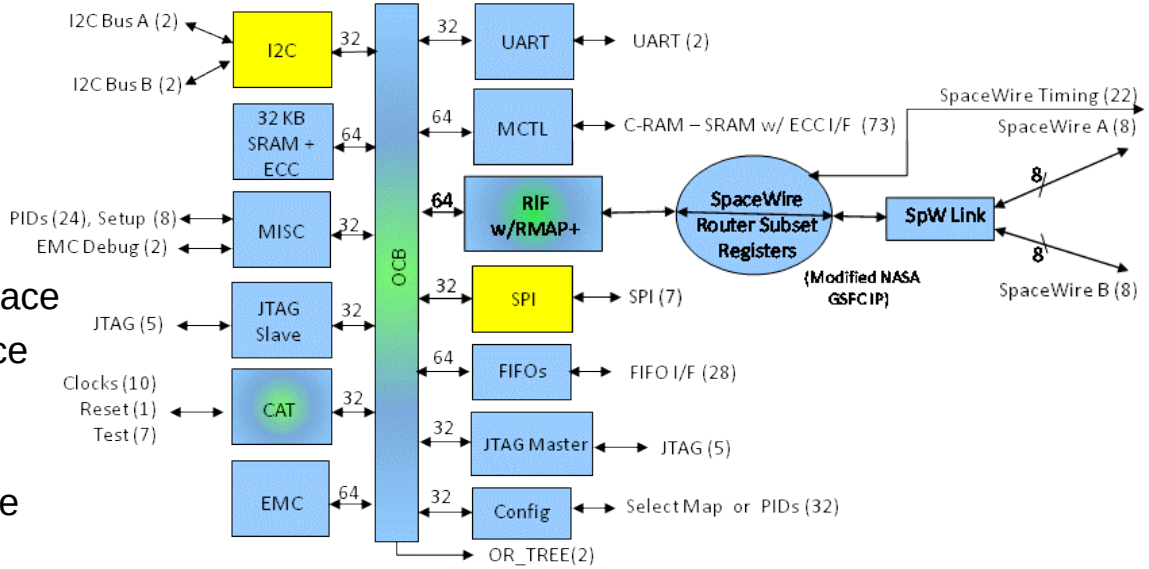
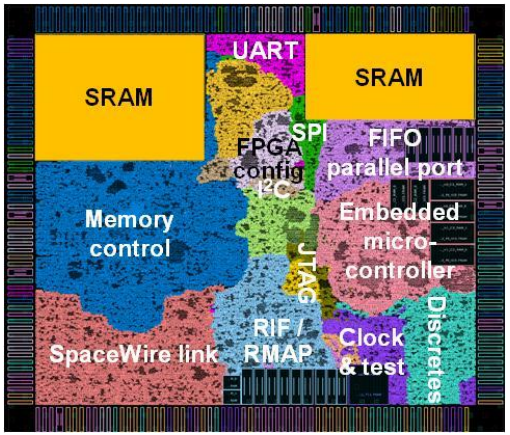
- **Features:**
  - Redundant single SpaceWire link with RMAP support @ 320 MHz / 256 Mb/s
  - 32-bit RISC controller capable of 15+ Dhrystone MIPS
  - 4 Master 1 Mbps Serial Peripheral Interface
  - Dual Inter-integrated circuit (I^2C) interface @ 100 to 400 Kb/s
  - External memory interface @ 3.2 Gb/s
  - RAM-based FPGAs Select Map interface
  - Plug and Play compatible
  - Extended network management features
  - Supplies: 1.5 V core, 3.3 V I/O;
  - Typical Power 0.1-1.4 W
- **Radiation resistance (projected):**
  - 1 Mrad (Si) Total Dose
  - <1e-10 upsets/bit-day SEU
  - Latch-up immune
- **Availability:** Die Fabricated in Test
  - Prototypes in 2 months





die layout

Versatile High Performance Low Power SpaceWire Endpoint ASIC

Embedded Microcontroller (EMC)

Block Diagram

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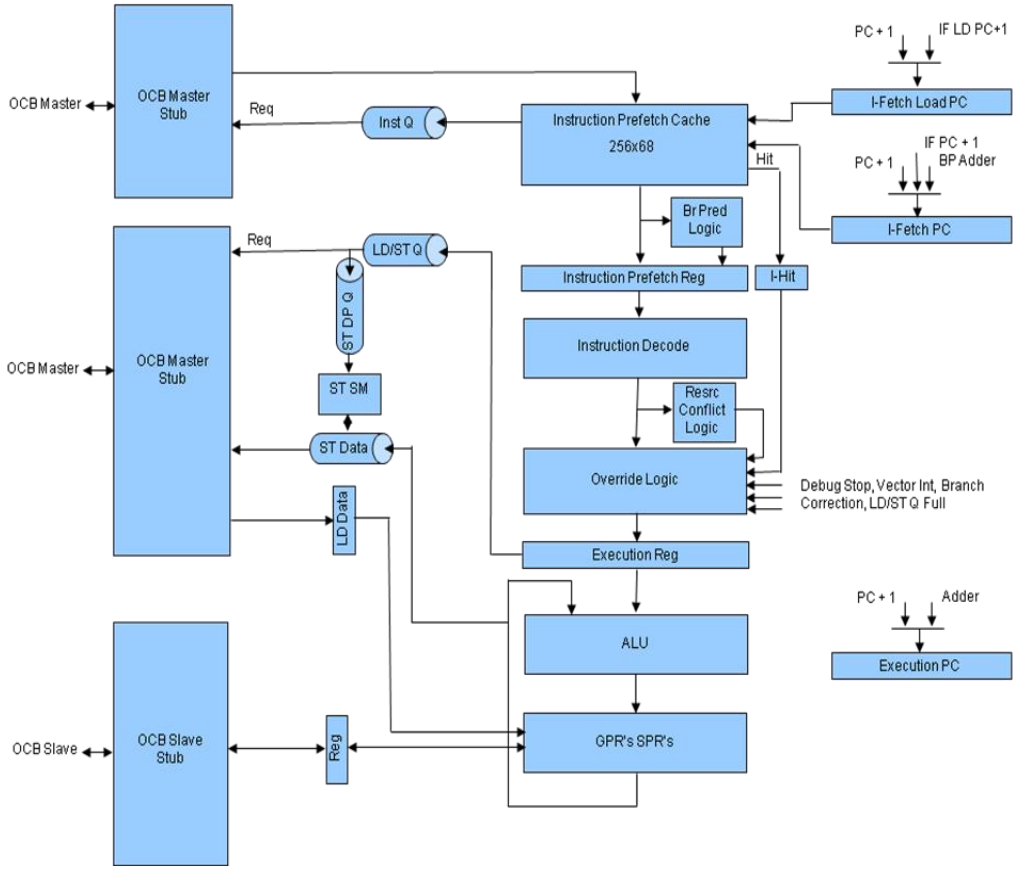

- Part of every BAE Systems Bridge or I/O ASIC
- Evolved from PAS
- 5 internal states
- 8 prioritized interrupts
- 6 forms of 32 bit instructions -> 46 different instructions
- Internal cache for instructions
- External stub for instructions and data
- Full set of support tools
  - C Compiler, assembler, linker, simulator

The EMC is a straightforward microcontroller which has been upgraded for instrument control applications and up to 16 Dhrystone MIPS performance

Golden Gate ASIC

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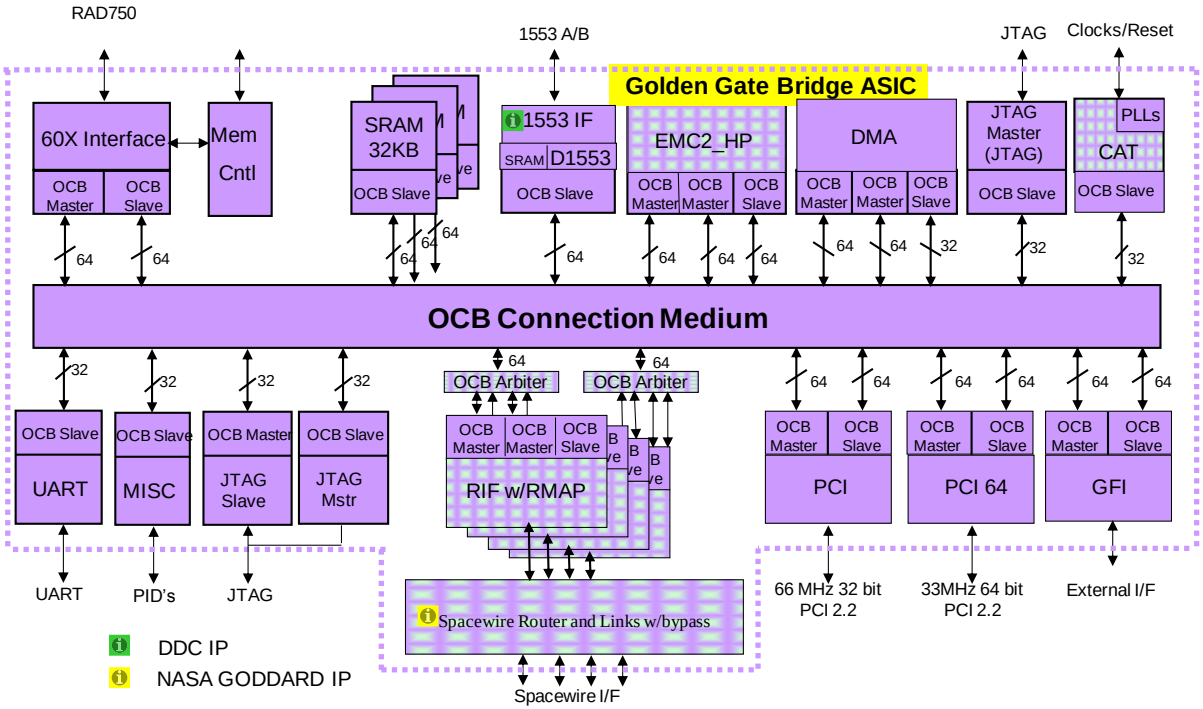

True SOC:

- **Latest EMC, DMA, Embedded Memory**
- **RAD750 Bridge ASIC**
- **4 Ports SpaceWire**
- **MIL-STD-1553B**
- **Dual PCI Bus**
- **Other Interfaces**

Golden Gate Bridge ASIC, the latest RAD750 companion interface chip or standalone instrument controller enables full system on a chip control and is working in the lab

Remote Memory Access Protocol (RMAP)

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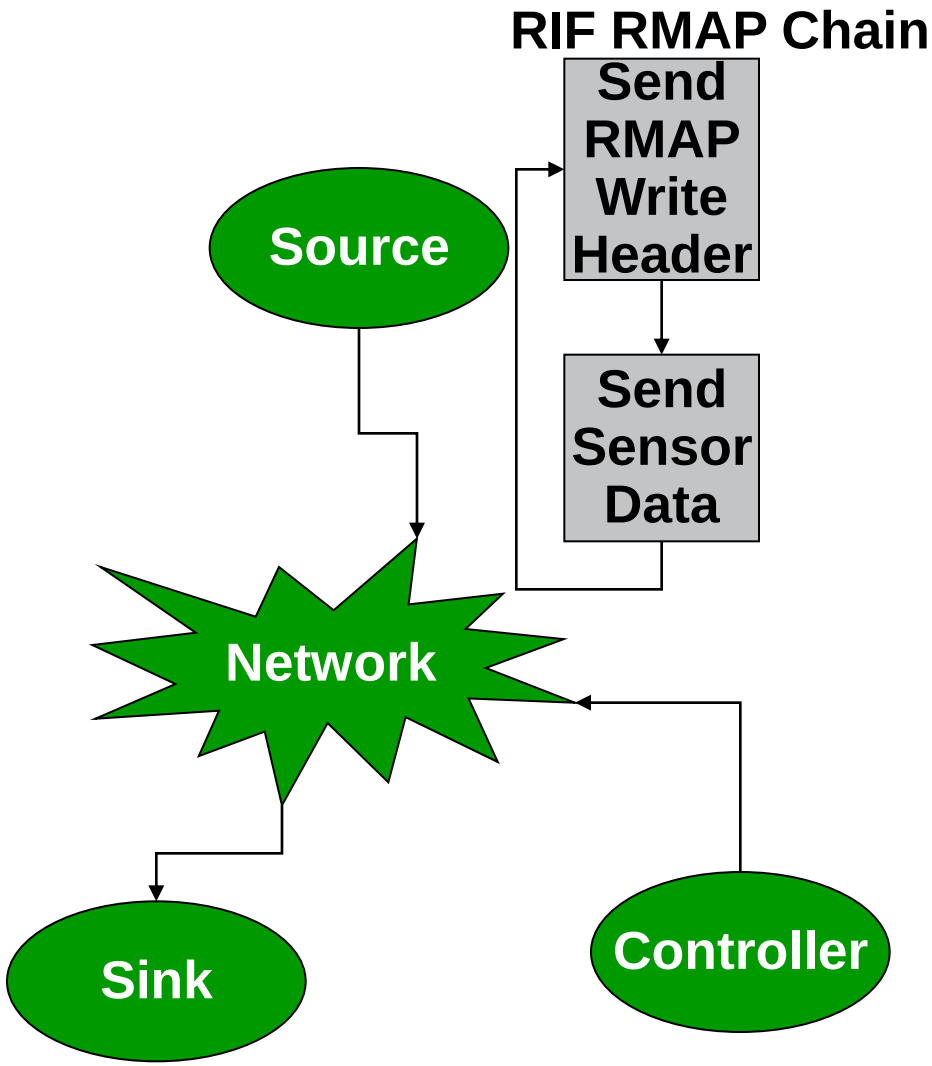
- RMAP is used extensively to configure and control the network and attached devices.
- It allows passive endpoints to be controlled by a central processor.
- By using the Router Interface (RIF) cores in our endpoints we can make passive endpoints autonomously communicate with other passive endpoints.
  - Controller uses RMAP to create RIF RMAP chains in Source Endpoint.
  - Controller uses RMAP to configure, start and stop the source and sink.



RMAP key to full utilization of SpaceWire in C&DH applications

SpaceWire Networks Core Improvements

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- RMAP capability added to RIF cores
  - Condensed External Port with RIF into one efficient structure
  - Enables memory mapped access to all core and OCB elements – typical C&DH usage
  - Included Bypass for direct access by Links – guaranteed transport
  - External Setup of Links and attached devices enabled – local intelligence now optional
  - All integrated into Golden Gate ASIC
- Identification Registers
  - Used for Network Management and recovery
  - Supports Network Discovery and node properties – multi-intelligence systems
- Byte and Packet Count Registers
  - Expanded RIF address space and added byte count registers
  - Expanded byte, normal and error end of packet count registers in each direction
  - Enables network diagnostics and instrumentation throughout network
- Latency Registers
  - Added RMAP addressable real time clock registers synced using timecodes
  - Added capture of receiver registers on receipt of write - enables hardware latency calculation
  - Can be used by software to measure time and/or confirm receipt of critical messages or data

These improvements enable better network management, diagnostics and measurements using built-in hardware features improving fault tolerance and network availability

Network Management

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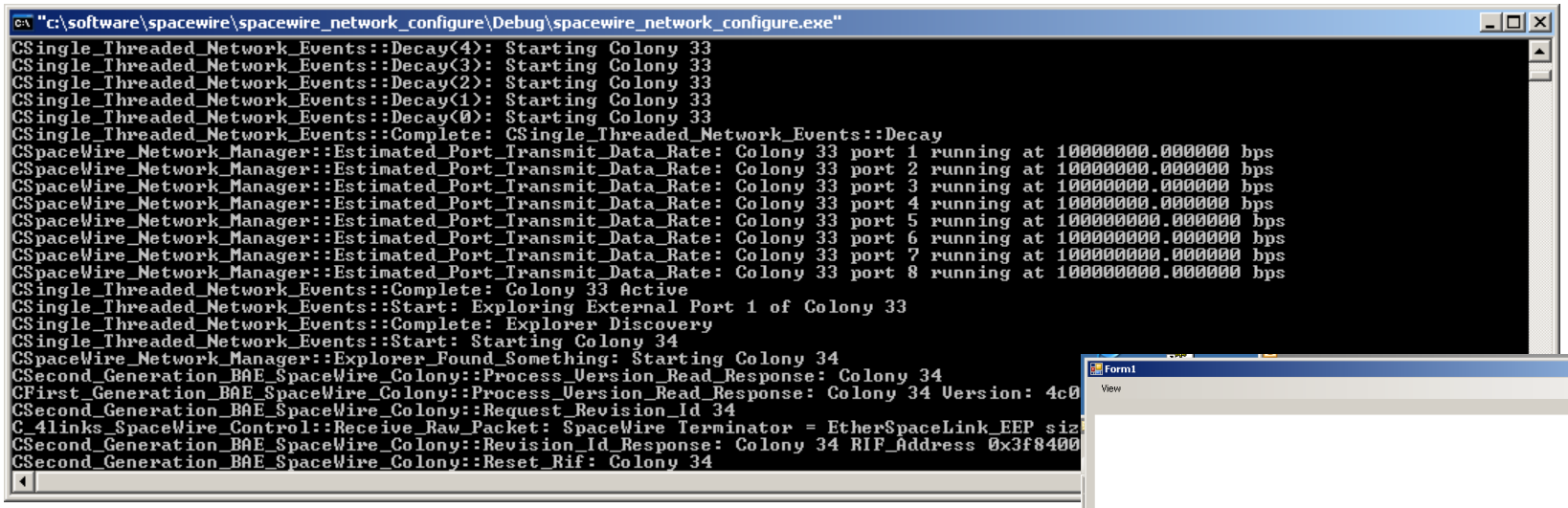

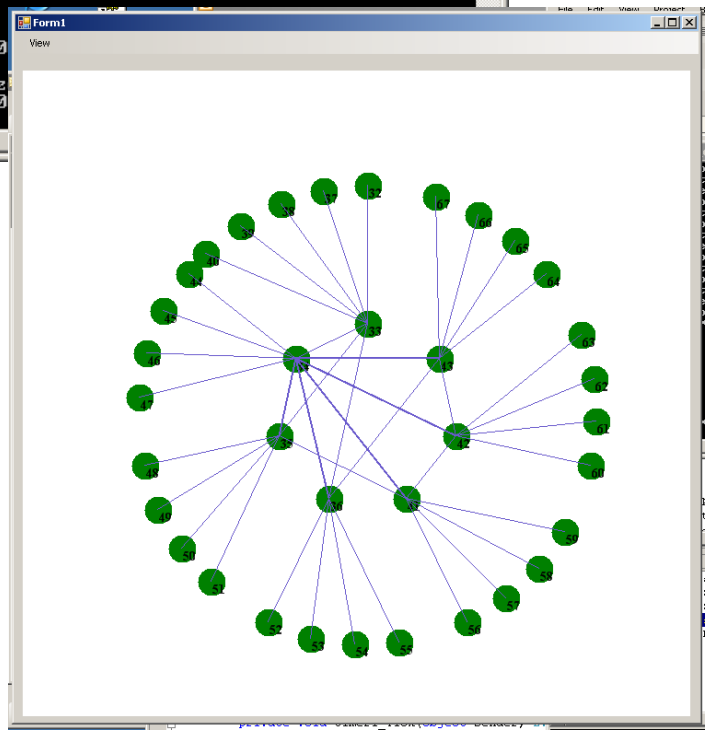

Software “Explores” Network by sending configuration messages through unexplored ports. If it finds something it records the device (and any ports it may have, and continues exploration.

Devices that are found are reported to the Monitor program for display

Wheel graphic at center of network information display

Application Management

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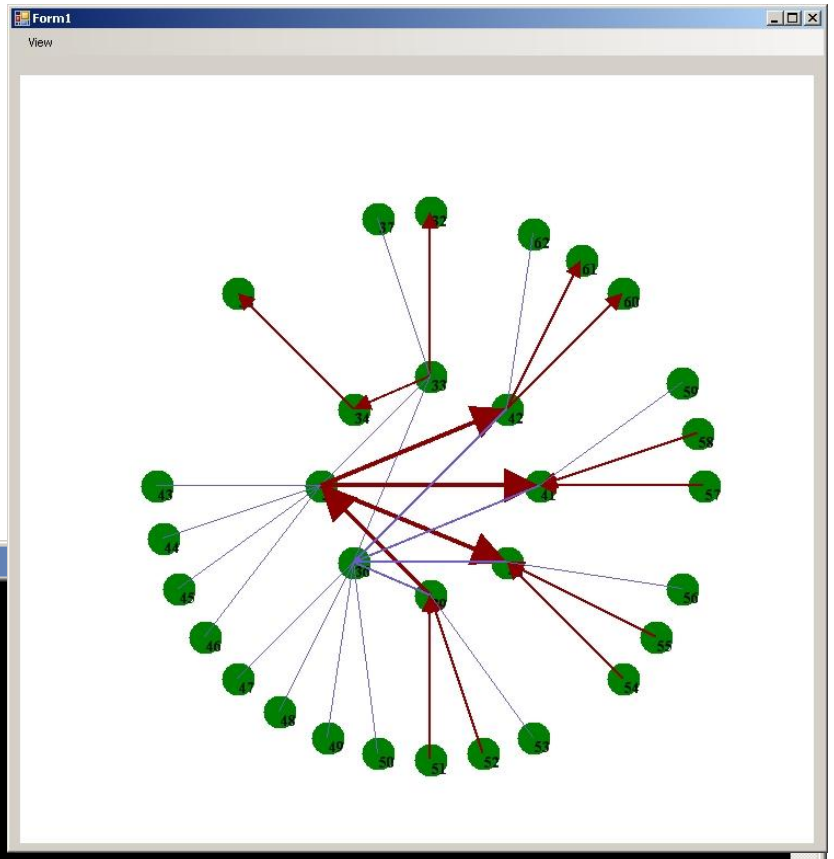
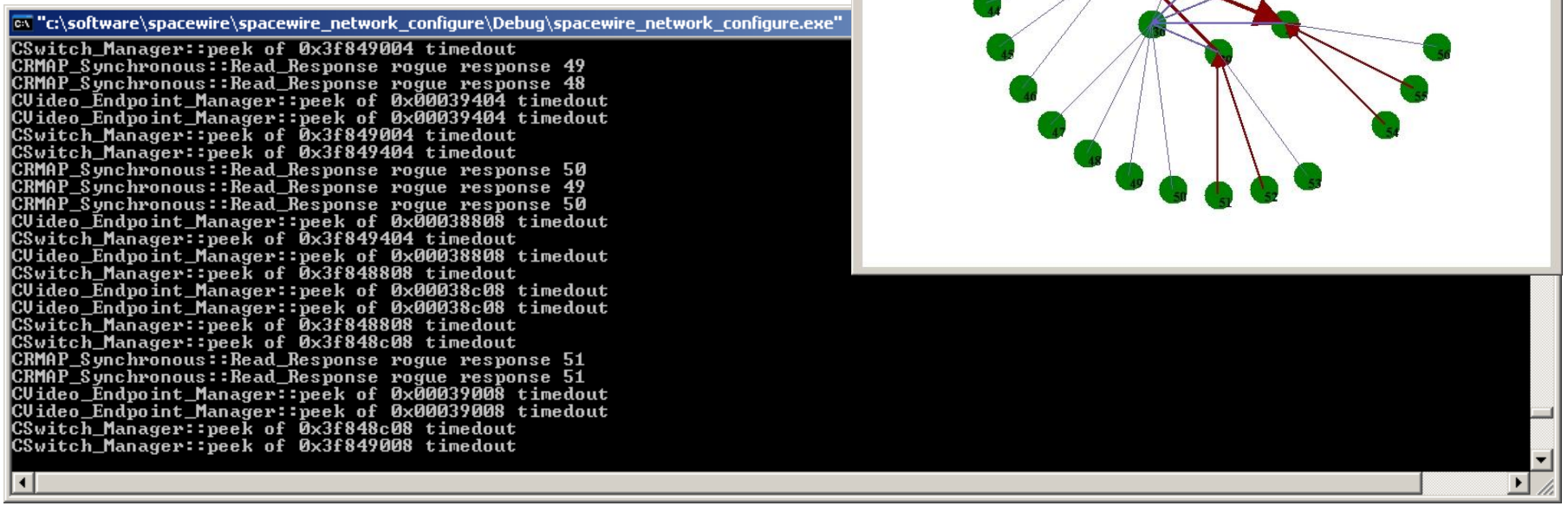
As devices are found and integrated into the network the application is informed of the device.

When sufficient resources are found the application configures the network and the devices to perform the mission.

This may be done automatically or on demand





Network Diagnostics

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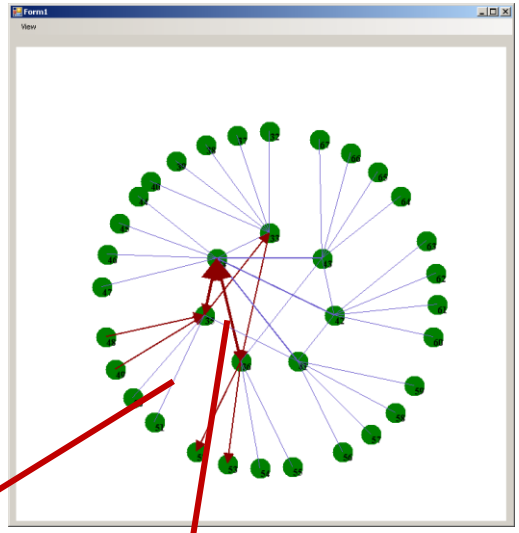
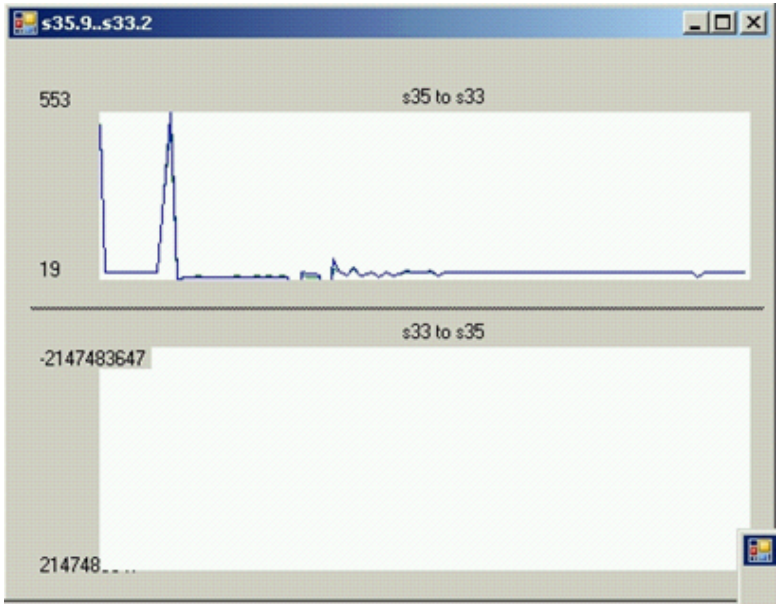
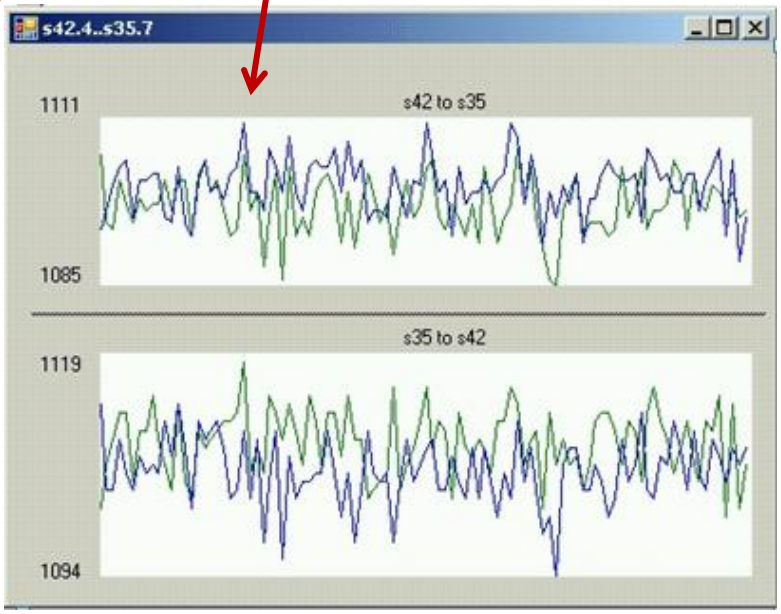
Each SpaceWire link may be selected to provide a view of its traffic in bytes, packets or errors.

This may be done automatically or on demand







Flight Application View of SpaceWire Software

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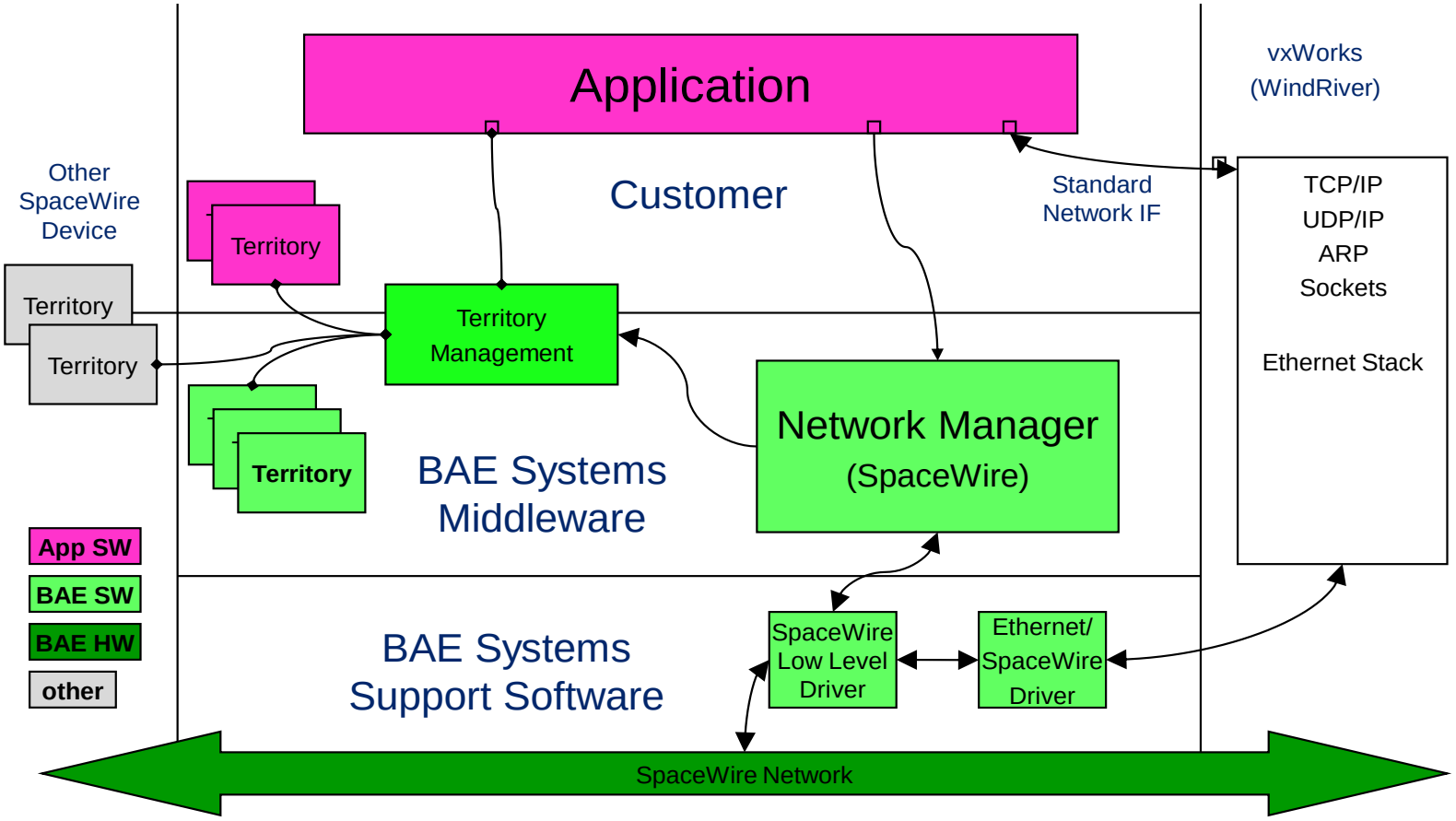

Low level drivers provided with SpaceWire components

Test and Debug over SpaceWire

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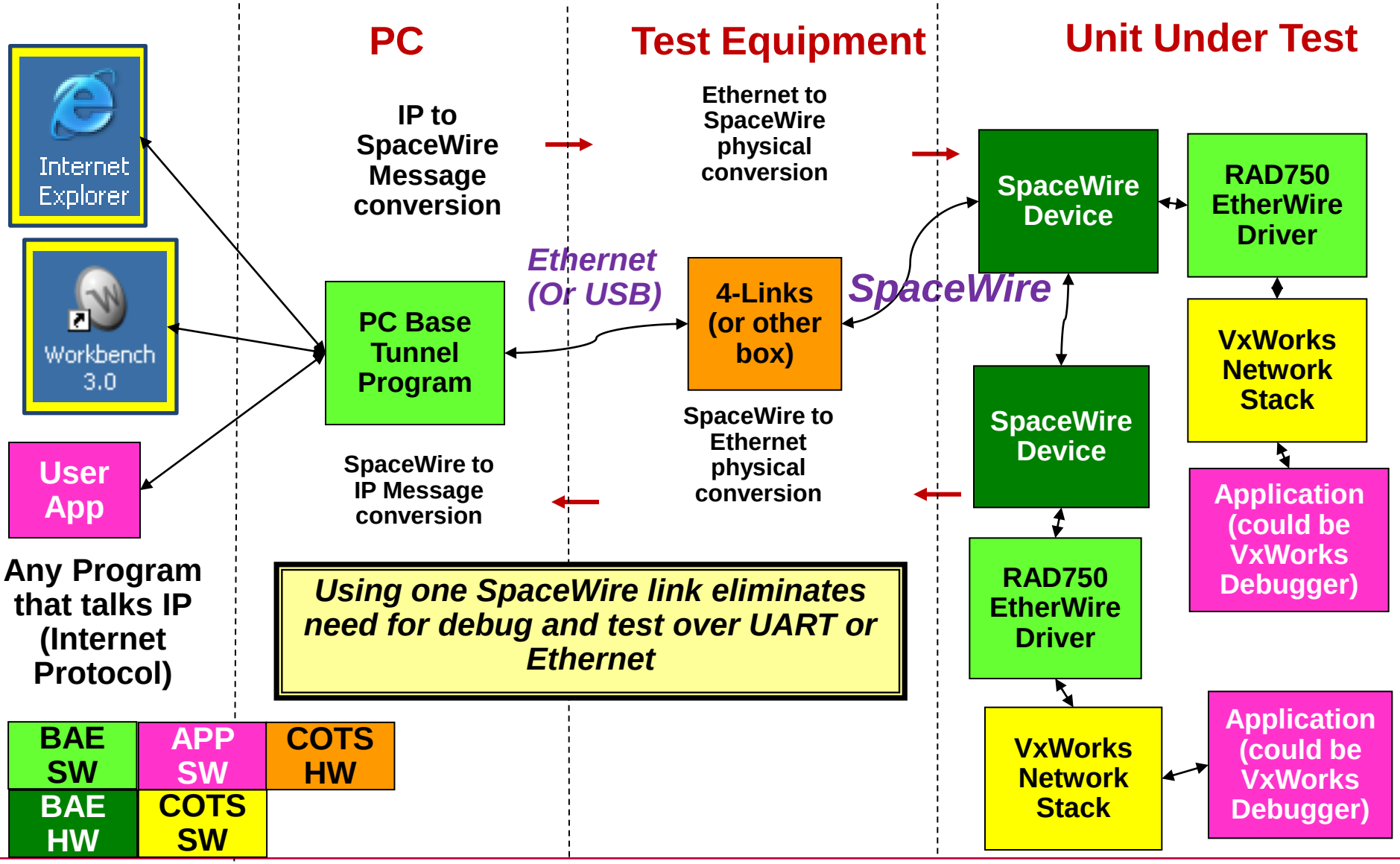

Summary

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- Shown SpaceWire Demonstration Laboratory Hardware and Software
- Enables new set of SpaceWire ASICs and Software
- Address SpaceWire applications in big and small systems
- Benchmark and demonstrate applications
- Stepping stone to SERDES based products