NGMP – Quad-core Next Generation Multipurpose Microprocessor with on-chip SpaceWire Router

www.aeroflex.com/gaisler

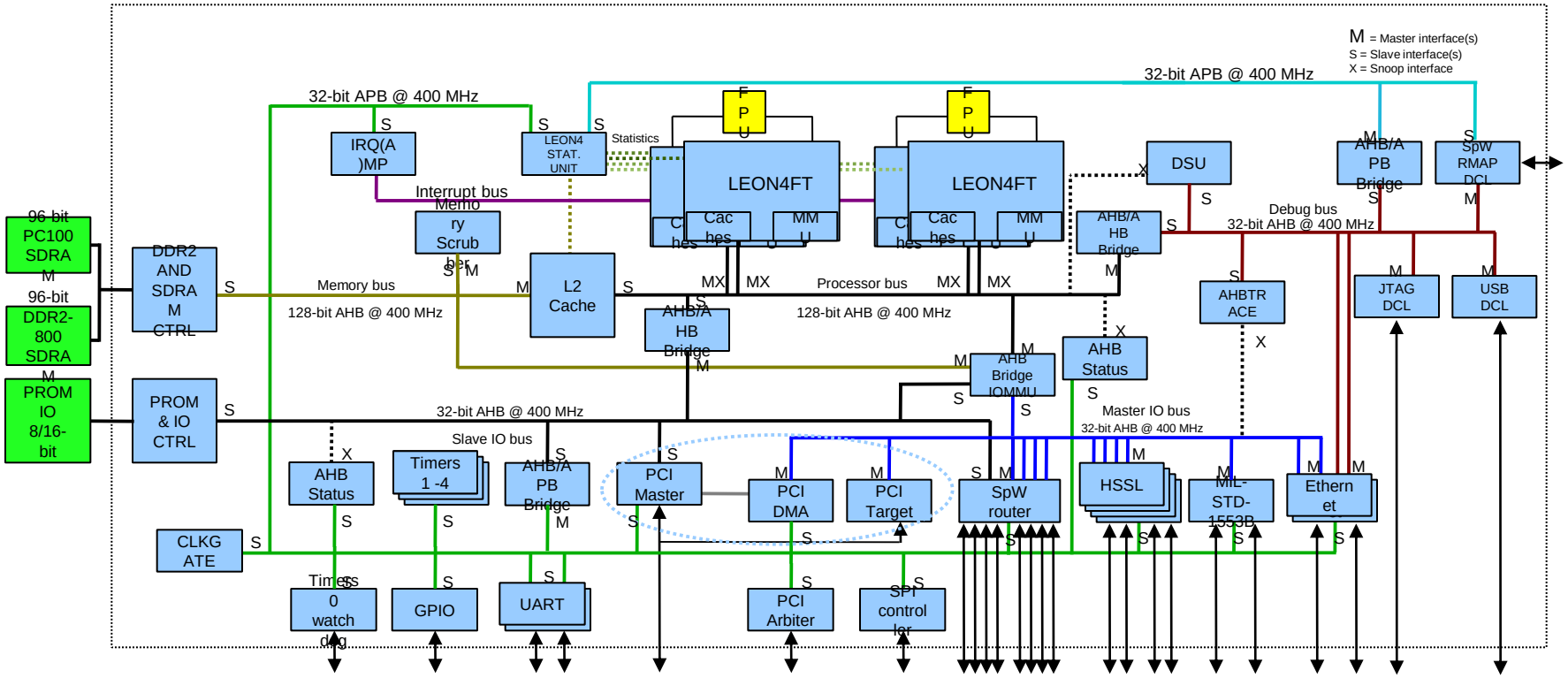
Overview

- NGMP is an ESA activity to develop a multi-core system with higher performance compared to earlier generations of European Space processors
- Part of the ESA roadmap for standard microprocessors
- Aeroflex Gaisler's assignment consists of specification, architectural design, verification by simulation and FPGA prototyping
- FPGA prototypes have been delivered
- Activity currently on hold in anticipation of progress on European space DSM technology, to resume 2012
- Meanwhile a functional prototype (FP) is developed

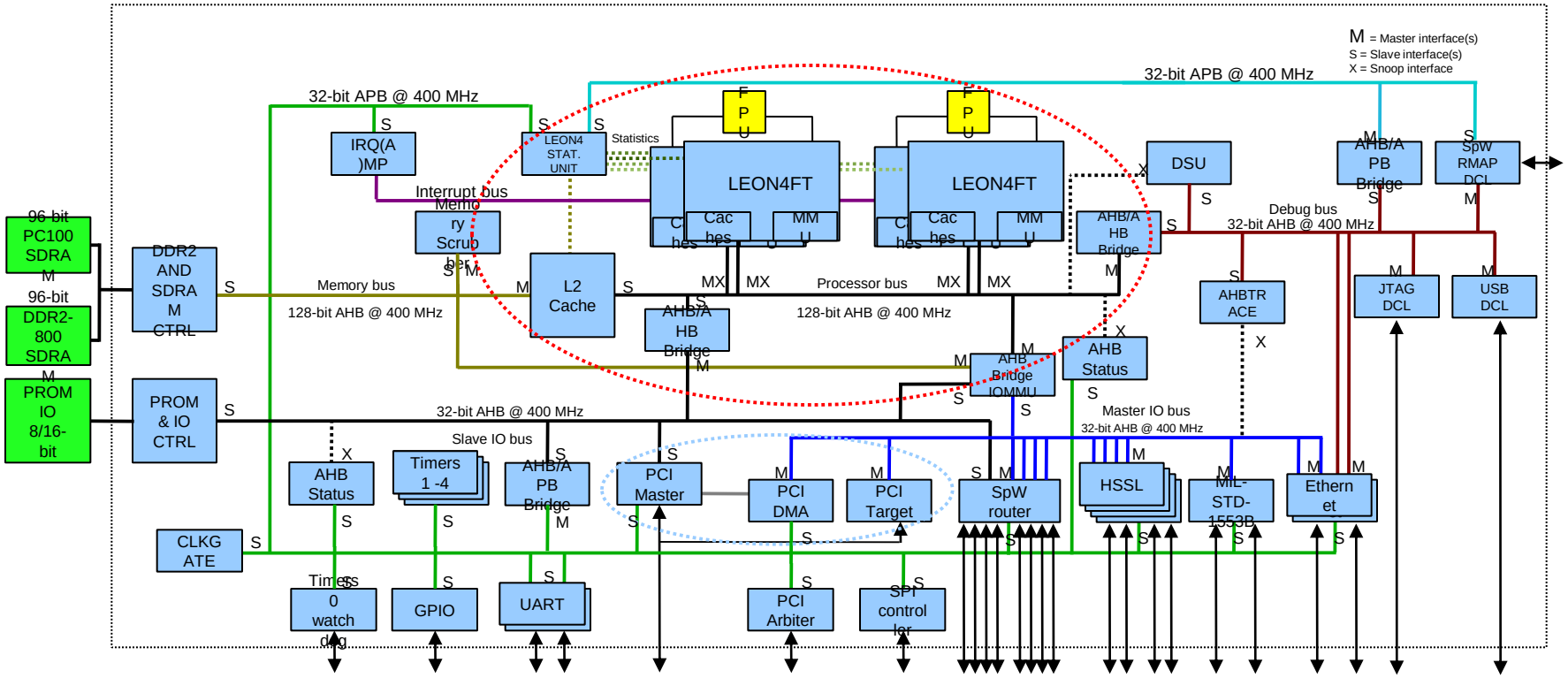
Architectural Overview

- Quad-core LEON4FT with two shared FPUs
- 128-bit L1 caches connected to 128-bit AHB bus
- 256+ KiB L2 cache, 256-bit cache line, 4-ways
- 64-bit DDR2-800/SDR-PC100 SDRAM memory interface
- 32 MiB on-chip DRAM (if feasible, not applicable for FP)
- 8-port SpaceWire router with four internal AMBA ports
- 32-bit, 66 MHz PCI interface
- 2x 10/100/1000 Mbit Ethernet
- 4x High-Speed Serial Links
- Debug links: Ethernet, JTAG, USB, SpW RMAP target
- 16x GPIO, SPI master/slave, MIL-STD-1553B, 2 x UART

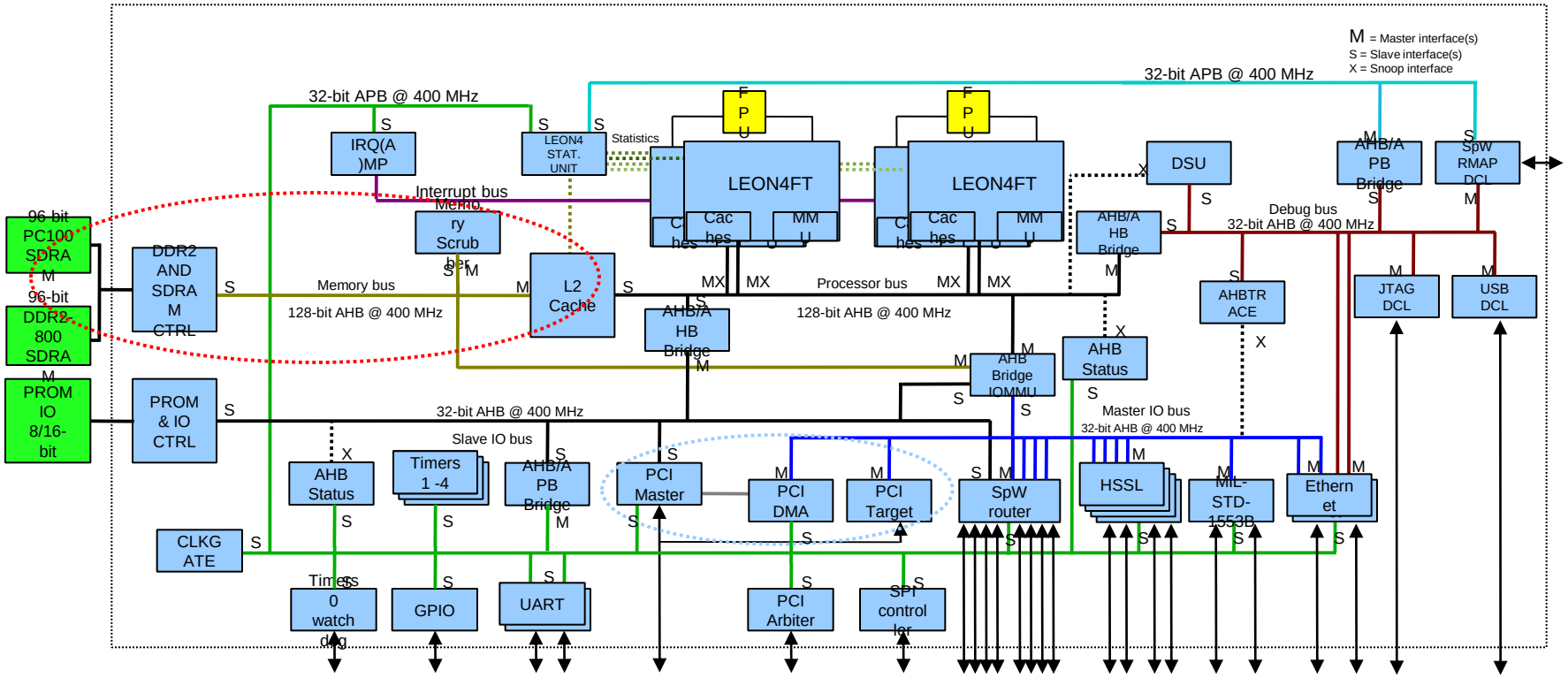
Architectural Overview



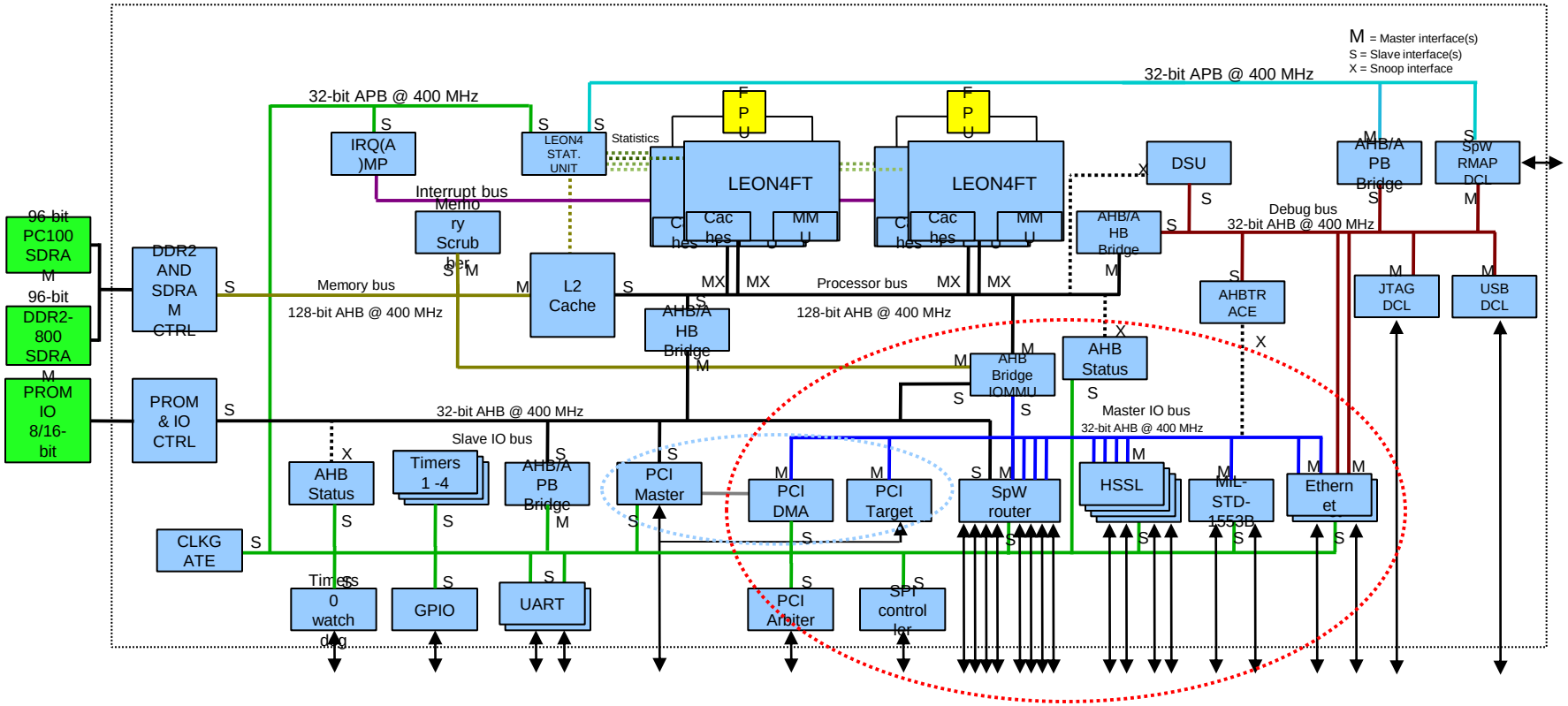
Architecture - Processor Bus



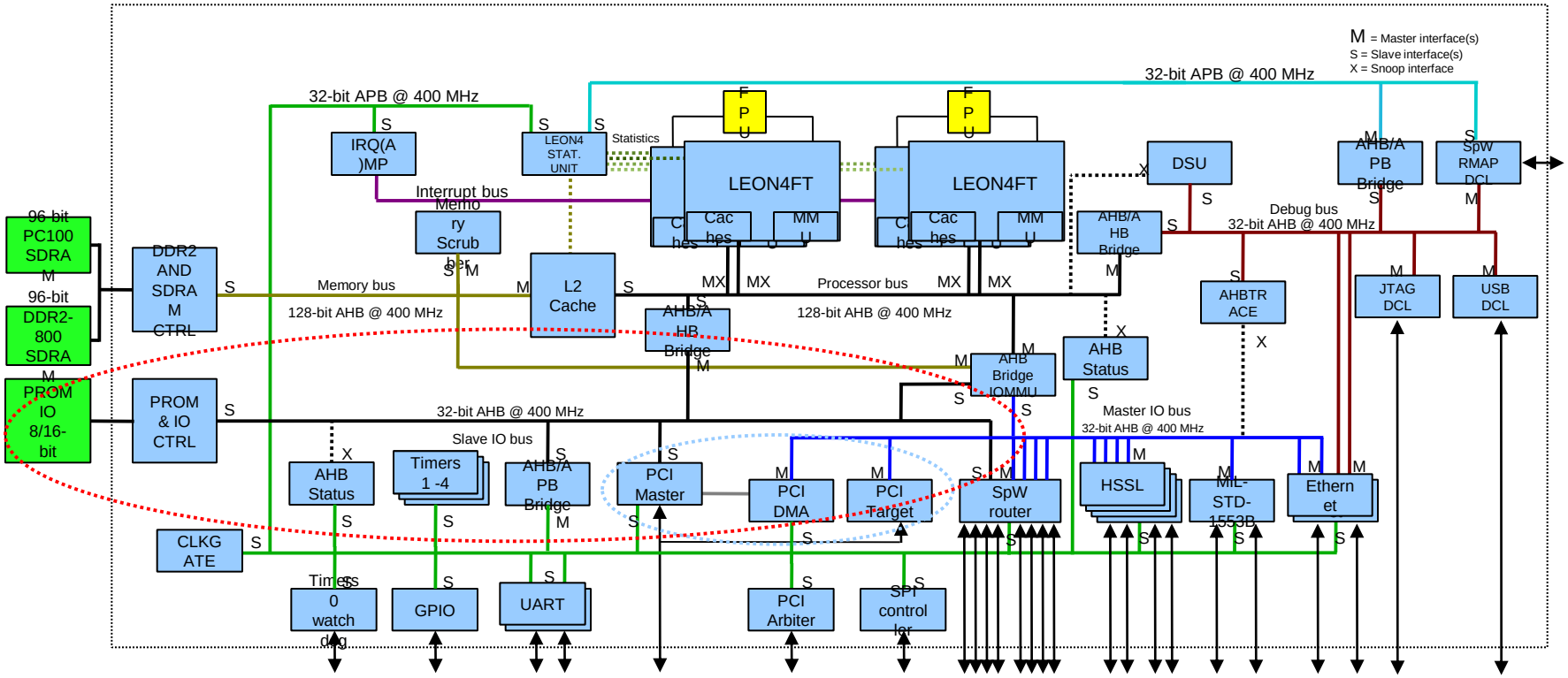
Architecture - Memory Bus



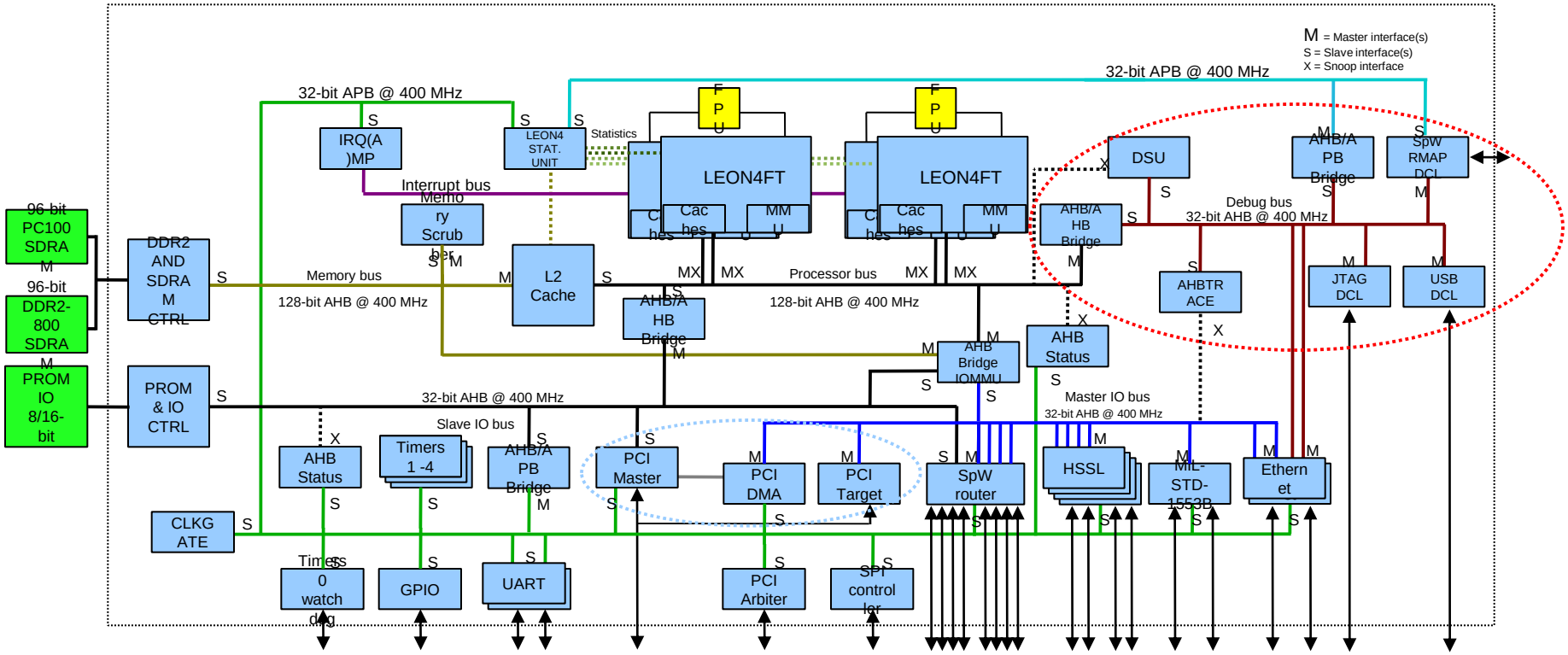
Architecture – Master I/O Bus



Architecture – Slave I/O Bus

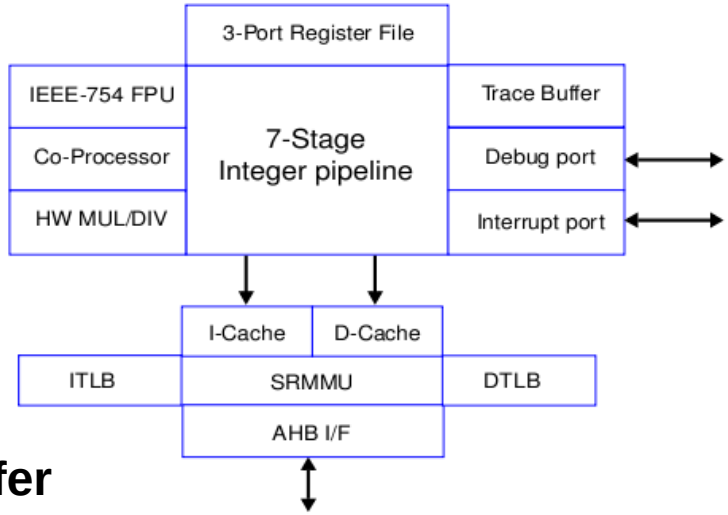


Architecture - Debug Bus



LEON4FT configuration

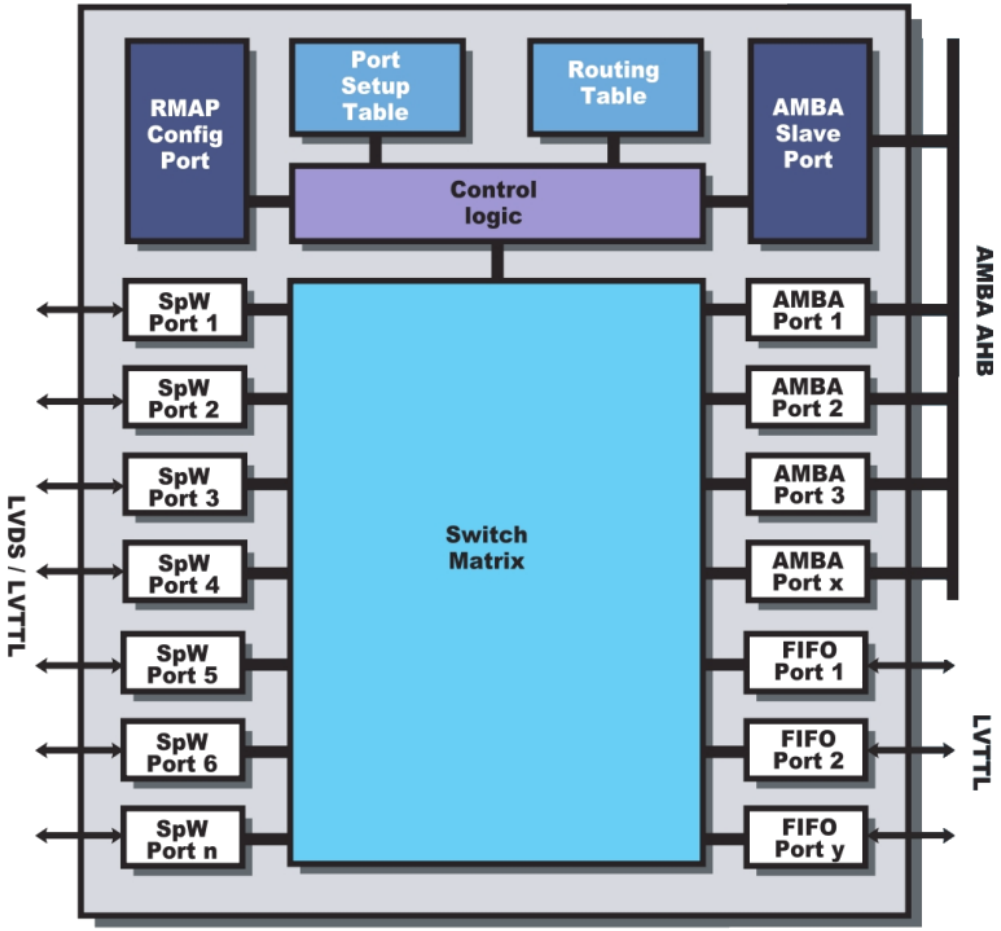
- IEEE-1754 SPARC V8 compliant 32-bit processor
- 7-stage pipeline, multi-processor support
- Separate multi-set L1 caches with LRU/LRR/RND, 4-bit parity
- 64-bit single-clock load/store operation
- 64-bit register file with BCH
- 128-bit AHB bus interface
- Write combining in store buffer
- Branch prediction
- CAS support
- Performance counters
- On-chip debug support unit with trace buffer
- 1.7 DMIPS/MHz, 0.6 Wheatstone MFLOPS/MHz
- Estimated 0.35 SPECINT/MHz, 0.25 SPECFP/MHz
- 2.1 CoreMark/MHz (comparable to ARM11)



SPARC Compliant SCD V8

SpaceWire router

- Aeroflex Gaisler GRSPWROUTER IP core
- 8 SpaceWire ports
- 4 internal AMBA ports
- 4 x 2 x 160 Mbps = 1,28 Gbps throughput towards AMBA bus
- Router is fully functional without processor intervention

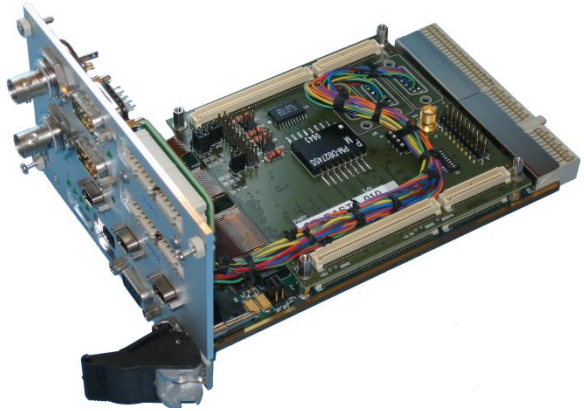


Target technology

- Baseline is ST 65 nm space technology
- Requirements:
  - 400 MHz system clock (i.e. 2720 DMIPS)
  - DDR2 PHY
  - I/O standards: LVTTL, SSTL, PCI
  - Memory: 1-port RAM, 2-port RAM
  - Memory: high density 1-port RAM/SDRAM
- Backup options:
  - UMC 90 nm with DARE library
  - Tower Jazz 130 nm with RadSafe library
- FP target technology: eASIC Nextreme2

Prototypes

- Full-speed functional prototype on evaluation board currently under development:
  - Will not include HSSL, nor large on-chip RAM
  - Includes DDR2 and SDR SDRAM on separate pins
- FPGA prototypes with reduced functionality available:
  - Xilinx ML510 and Synopsys HAPS-51
  - Aeroflex Gaisler GR-CPCI-XC4V with LX200 FPGA
  - Aeroflex Gaisler GR-PCI-XC5V



Current status / Schedule

NGMP ASIC activity

- **Aug 2009: Kick-off**
- **Feb 2010: Definition and specification**
- **June 2010: First versions of FPGA prototypes**
- **Dec 2010: Final RTL code, FPGA demonstrator**
- **Aug 2011: Verified ASIC netlist (postponed)**

NGMP functional prototype activity

- **May 2011: Kick-off**
- **July 2011: Definition and specification**
- **Nov 2011: Architectural and detailed design**
- **Jan 2012: Layout generation and verification**
- **May 2012: Prototype implementation, validation**
- **Q2 2012: Prototypes on evaluation board**